Version 2
This version confirms that there will be no further January assessments.

GCE

Examinations from 2009

First AS Award: Summer 2009

First A Level Award: Summer 2010

Electronics

Contents

WJEC AS GCE in Electronics
WJEC A Level GCE in Electronics

First AS Award - Summer 2009
First A level Award - Summer 2010

GCE Electronics

Subject/Option Entry Codes	
Advanced Subsidiary (AS) "Cash in" entry *A Level (A)"Cash in" entry*	*2141* *3141*
ET1 : Introduction to Digital and Analogue Systems	1141
ET2 : Electronic Circuits and Components	1142
ET3 : Programmable Control Systems Project	1143
ET4 : Electronic Communications Systems	1144
ET5 : Electronic Systems Applications	1145
ET6 : Electronic Design Project	1146

When making entries, the following option codes should be entered after the four digit unit or cash-in code to indicate English medium or Welsh medium entries:

English medium 01
Welsh medium W1

Availability of Assessment Units			
Unit	**January 2009**	**June 2009**	**June 2009 & each subsequent year**
ET1	✓	✓	✓
ET2		✓	✓
ET3		✓	✓
ET4			✓
ET5			✓
ET6			✓

Qualification Accreditation Numbers

Advanced Subsidiary: 500/2796/7
Advanced: 500/2606/9

SUMMARY OF ASSESSMENT

This specification is divided into a total of 6 units: 3 AS units and 3 A2 units. Weightings noted below are expressed in terms of the full A level qualification.

AS (3 units)

ET 1	17.5% 1¼ hour Written Paper 60 marks [105 UM]
Introduction to Digital and Analogue Systems Approximately 8 questions. No question choice. No sections	
ET2	17.5% 1¼ hours Written Paper 60 marks[105 UM]
Circuits and Components Approximately 8 questions. No question choice. No sections	
ET3	15% Internal Assessment 40 marks [UMS = 90]
Programmable Control Systems Project To design and test two programs for systems control: 1 high-level language [Ladder logic] and 1 assembler language. 40 raw marks.	

A LEVEL (the above plus a further 3 units)

ET4	15% 1 hour Written Paper 50 marks [90 UM]
Communications Systems Approximately 7 questions. No question choice. No sections	
ET5	20% 1½ hour written paper 70 marks [120 UM]
Systems Applications Approximately 9 questions. No question choice. No sections	
ET6	15% Internal Assessment 50 marks [90 UM]
Design Project To design, realise and test an electronic system to meet a specified problem of the candidate's choosing. 40 raw marks.	

All assessment units are available in June.

Synoptic Assessment is included in ET4 and ET5 and is inherent in the Design Project ET6.

Electronics

1 INTRODUCTION

1. 1 Criteria for AS and A Level GCE

This specification has been designed to meet the general criteria for GCE AS (AS) and A Level (A) and the subject criteria for AS/A Electronics as issued by the regulators [July 2006]. The qualifications will comply with the grading, awarding and certification requirements of the Code of Practice for 'general' qualifications (including GCE).

The AS qualification will be reported on a five-grade scale of A, B, C, D, E. The A level qualification will be reported on a six-grade scale of A*, A, B, C, D, E. The award of A* at A level will provide recognition of the additional demands presented by the A2 units in term of 'stretch and challenge' and 'synoptic' requirements. Candidates who fail to reach the minimum standard for grade E are recorded as U (unclassified), and do not receive a certificate. The level of demand of the AS examination is that expected of candidates half way through a full A level course.

The AS assessment units will have equal weighting with the second half of the qualification (A2) when these are aggregated to produce the A level award. AS consists of three assessment units, referred to in this specification as ET1, ET2 and ET3. A2 also consists of three units and these are referred to as ET4, ET5 and ET6.

Assessment units may be retaken prior to certification for the AS or A level qualifications, in which case the better result will be used for the qualification award. Individual assessment unit results, prior to certification for a qualification, have a shelf-life limited only by the shelf-life of the specification.

The specification and assessment materials are available in English and Welsh.

1.2 Prior learning

There are no specific entry qualifications for this specification. It is suitable for students with a wide range of educational backgrounds and for all ages. The specification builds upon the knowledge, understanding and skills set out in the National Curriculum Key Stage 4 programme of study for GCSE Science. It also assumes knowledge, to GCSE standard, of the following quantities associated with current electricity, the relationships between them and the SI units in which they are measured:
voltage, current, resistance and power.

1.3 Progression

The six-part structure of this specification (3 units for AS, and an additional 3 for the full Advanced) allows for both staged and end-of-course assessment and thus allows candidates to defer decisions about progression from AS to the full A level qualification.

This specification provides a suitable foundation for the study of Electronics or a related area through a range of higher education courses (e.g. Electronics, Engineering, Physics) or direct entry into employment. In addition, the specification provides a coherent, satisfying and worthwhile course of study for candidates who do not progress to further study in this subject.

1.4 Rationale

The specification for AS and A-level Electronics complies with the GCE AS and A Subject Criteria for Science Subjects, published by CCEA, DELLS and QCA. It provides

(a) a complete course in Electronics to GCE A level;

(b) a firm foundation in Electronics knowledge and understanding, together with mathematical competence for those wishing proceed to further studies in Electronics, Engineering or the Natural Sciences;

(c) encouragement to candidates to develop skills of analysis, evaluation and research as well as the ability of critical thinking in terms of the applications of Electronics to contemporary issues.

(d) opportunities for candidates to develop key skills in the areas of Communication, Application of Number and Information Technology.

1.5 The Wider Curriculum

Electronics is a subject that by its nature requires candidates to consider individual, moral, ethical, social, cultural and contemporary issues. The mass production of electronic products and the use of electronics in control systems present citizens with a plethora of choice and moral questions. Electronic systems play a large part in attempts by society to co-exist with nature in the long term. The specification provides opportunities for candidates to develop an understanding of such issues as they relate to the designer, manufacturer or user of electronic devices.

The internally-assessed units ET3 and ET6, based upon the design and production of programs and devices, encourage the consideration of social, ethical and moral influences on the purpose, design, production and testing of products. Candidates may be encouraged to develop a balanced appreciation of the conflicts and dilemmas involved in the design and manufacture of products or systems. In designing, testing and developing their systems, ET6 candidates are expected to address Health and Safety issues.

1.6 Prohibited combinations and overlap

Every specification is assigned a national classification code indicating the subject area to which it belongs. Centres should be aware that candidates who enter for more than one GCE qualification with the same classification code will only have one grade (the highest) counted for the purpose of the School and College Performance Tables. The classification code for this specification is 1730.

This specification does not overlap significantly with any other, although there will be elements of overlap, for example, with Physics. There are no prohibited combinations.

1.7 Equality and Fair Assessment

AS/A levels often require assessment of a broad range of competences. This is because they are general qualifications and, as such, prepare candidates for a wide range of occupations and higher level courses.

The revised AS/A level qualification and subject criteria were reviewed to identify whether any of the competences required by the subject presented a potential barrier to any disabled candidates. If this was the case, the situation was reviewed again to ensure that such competences were included only where essential to the subject. The findings of this process were discussed with disability groups and with disabled people.

In *GCE Electronics* practical assistants may be used for manipulating equipment and making observations. Technology may help visually impaired students to take readings and make observations.

Reasonable adjustments are made for disabled candidates in order to enable them to access the assessments. For this reason, very few candidates will have a complete barrier to any part of the assessment. Information on reasonable adjustments is found in the Joint Council for Qualifications document *Regulations and Guidance Relating to Candidates who are eligible for Adjustments in Examinations.* This document is available on the JCQ website (www.jcq.org.uk).

Candidates who are still unable to access a significant part of the assessment, even after exploring all possibilities through reasonable adjustments, may still be able to receive an award. They would be given a grade on the parts of the assessment they have taken and there would be an indication on their certificate that not all of the competences have been addressed. This will be kept under review and may be amended in future.

2 AIMS

The AS and A specifications in Electronics aim to encourage students to:

(a) develop an enthusiasm for Electronics and, where appropriate to pursue this enthusiasm in its further study;
(b) appreciate the role of Electronics in society, in particular how electronics is applied and how decisions about its use are made;
(c) appreciate the interconnectedness of the subject and the ways in which different strands of Electronics can be used jointly to solve problems;
(d) develop an understanding of the social processes of Electronics as a subject with a basis in experimental science and applications in modern technology;
(e) acquire a more general understanding of the way in which scientific disciplines make progress, acquire and interpret evidence, propose and evaluate solutions, communicate ideas and interact with society, as outlined in section 3.6, *How Science Works*, of the GCE AS and A level criteria for Science Subjects.

How science Works

A further aim of the AS and A specifications in Electronics is to encourage students to understand ***How Science Works***. In the context of AS/A Electronics, this means that candidates should:

- use knowledge and understanding to pose questions, define problems, present scientific arguments and ideas;
- use appropriate methodology, including ICT, to answer questions and solve problems;
- carry out experimental and investigative activities, including appropriate risk management, in a range of contexts;
- analyse and interpret data to provide evidence, recognising correlations and causal relationships;
- evaluate methodology, evidence and data, and resolve conflicting evidence;
- communicate information and ideas in appropriate ways using appropriate terminology;
- consider applications and implications of electronics and appreciate their associated benefits and risks;
- appreciate the ways in which society uses electronics to inform decision-making.

3 ASSESSMENT OBJECTIVES

Candidates must meet the following assessment objectives in the context of the content detailed in Section 4 of the specification:

AO1: **Knowledge and understanding of science and of *How science works***

Candidates should be able to:

(a) recognise, recall and show understanding of scientific knowledge
(b) select, organise and communicate relevant information in a variety of forms.

AO2: Application of knowledge and understanding of science and of *How science works*

Candidates should be able to:

(a) analyse and evaluate scientific knowledge and processes
(b) apply scientific knowledge and processes to unfamiliar situations including those related to issues
(c) assess the validity, reliability and credibility of scientific information.

AO3: *How science works*

Candidates should be able to:

(a) demonstrate and describe ethical, safe and skilful practical techniques and processes, selecting appropriate qualitative and quantitative methods.
(b) make, record and communicate reliable and valid observations and measurements with appropriate precision and accuracy.
(c) analyse, interpret, explain and evaluate the methodology, results and impact of their own and others' experimental and investigative activities in a variety of ways.

Weightings

Assessment objective weightings are shown below as % of the full A level, with AS weightings in brackets.

Unit	Raw marks allocation				% unit weighting
	unit total	AO1	AO2	AO3	
ET1	**60**	**26**	**30**	**4**	**17.5 (35)**
ET2	**60**	**26**	**30**	**4**	**17.5 935)**
ET3	**40**	**9**	**3**	**28**	**15 (30)**
ET4	**50**	**18**	**29**	**3**	**15**
ET5	**70**	**26**	**40**	**4**	**20**
ET6	**50**	**5**	**5**	**35**	**15**

Total AS%	**37**	**37**	**26**
Total A2%	**28**	**46**	**26**
Total A%	**33**	**42**	**26**

4 SPECIFICATION CONTENT

4.1 Units

SI units will be used throughout this specification. Knowledge of the following SI multiples and sub-multiples will be required:
G, M, k, μ, n and p

4.2 Practical Work

Practical work will play an important role throughout the course. It is assumed that candidates will be familiar with appropriate test instruments and safe operating practices as outlined in relevant DATA / ASE / CLEAPSS documents.

4.3 Mathematical requirements

Candidates will be required to:

4.3.1 Computation

- recognise and use expressions in decimal and standard form
- use ratios, fractions and percentages;
- use calculators to find and use power, exponential and logarithmic functions;
- use calculators to handle sin *x,* cos *x,* tan *x* when *x* is expressed in degrees or radians;
- use hexadecimal and binary systems;

4.3.2 Algebra

- understand and use the symbols: =, <, ≪, ≫,>, ∝, ~;
- change the subject of an equation;
- substitute numerical values into algebraic equations using appropriate units for physical quantities;
- solve simple algebraic equations;

4.3.3 Graphs

- translate information between graphical, numerical and algebraic forms;
- plot two variables from experimental or other data;
- determine the slope and intercept of a linear graph;
- draw and use the slope of a tangent to a curve as a measure of rate of change.

4.4 Use of IT

The use of IT should pervade the course. Opportunities are available for modelling systems, circuit simulation and the use of graphic interfaces for programming tasks in the two internally assessed units. Project reports will also make use of ICT.

AS

UNIT ET1 – Introduction to Analogue and Digital Systems.

AREA OF STUDY		*AMPLIFICATION*
		Candidates should be able to:
1.1 Logic gates		
1.1.1	Types of logic gates	identify and use NOT, AND, NAND, OR, NOR, EXOR, XNOR gates; construct and recognise truth tables for these gates and simple combinations of them, with up to 4 inputs;
1.1.2	Simple digital inputs	recall the use of mechanical switches with resistors and pulse generators to provide inputs for logic systems; explain the consequences of floating inputs and the use of pull-up and pull-down resistors;
1.1.3	Simple digital outputs	recall the use of an LED and resistor to indicate the output state of a logic system; understand that a logic gate output can be configured to either source or sink current;
1.2 Logic system design		
1.2.1	Logic System Specification	translate a specification into a truth table; design and test a system, with up to 4 inputs from a specification;
1.2.2	System simplification using Boolean algebra	generate the Boolean expression for a system [with up to 3 inputs] from a truth table; generate the Boolean expression for a system [with up to 4 inputs] from a logic diagram; recall and use the following: • $A.1=A$ • $A.0=0$ • $A.\overline{A}=0$ • $A+1=1$ • $A+0=A$ • $A+\overline{A}=1$ select and use the following: • $A+\overline{A}.B = A+B$ • $A.B+A=A(B+1)=A$; apply DeMorgan's theorem to simplify a logic system [with up to 3 inputs];
1.2.3	System simplification using Karnaugh mapping	draw a Karnaugh map for a logic system with up to 4 inputs and use it to minimise the number of gates required;

AREA OF STUDY		***AMPLIFICATION***
		Candidates should be able to:
1.2.4	NAND gate logic	use combinations of NAND gates to perform other logic functions; implement a logic system using only NAND gates; recognise redundant gates in such a system.
1.2.5	System simplification using multiplexers	design and analyse a system with up to 4 inputs using a multiplexer as a programmable logic system;
1.3	**Sequential logic systems**	
1.3.1	Bistables	design a Set-Reset latch based on NAND gates; use a truth table sequence to describe the action of such bistables;
1.3.2	D-type flip-flops	draw a timing diagram to illustrate the significance of edge triggering; draw a timing diagram to illustrate how a transition gate can be used to produce edge-triggering; distinguish between the operation of the clocked data input and the set/reset inputs on a D-type flip-flop; design a transition gate to a given specification;
1.3.3	Counters	connect a series of D-type flip-flops or counters to produce a frequency divider circuit: design 4-bit up and down counters based on D-type flip-flops; design 4-bit modulo-n counters and binary coded decimal (BCD) counters; draw timing diagrams for these counters; describe the use of decoders and seven-segment displays; convert between binary, decimal and BCD number systems; design systems that use a counter and combinational logic to produce a sequence of events;
1.4	**Operational amplifiers**	
1.4.1	Op amp characteristics	recall the following characteristics of an ideal op-amp: • infinite open loop gain • infinite input impedance • zero output impedance • infinite slew-rate • infinite common-mode rejection ratio; interpret these characteristics given data for a specific op amp;

AREA OF STUDY		***AMPLIFICATION***
		Candidates should be able to:
1.4.2	Inverting amplifier	draw and recognise the inverting amplifier circuit; design an inverting amplifier using resistive negative feedback to achieve specified voltage gain; select and use the formulae $G = \frac{V_{OUT}}{V_{IN}} = -\frac{R_F}{R_{IN}}$; use the approximation that the input impedance is equal to the resistance of the input resistor.
1.4.3	Non-inverting amplifier	draw and recognise the non-inverting amplifier circuit; design a non-inverting amplifier using resistive negative feedback to achieve specified voltage gain; select and use the formulae $G = \frac{V_{OUT}}{V_{IN}} = 1 + \frac{R_F}{R_1}$ know that the input impedance is equal to that of the op-amp;
1.4.4	Bandwidth	know that the bandwidth is the frequency range over which the voltage gain is greater than $1/\sqrt{2}$ of its maximum value; estimate this bandwidth from a frequency response curve; use the gain-bandwidth product (unity gain bandwidth) to estimate bandwidth;
1.4.5	Practical voltage amplifiers	draw and interpret graphs of the response of inverting and non-inverting amplifiers to AC and DC input signals; design single stage amplifiers based on inverting or non-inverting voltage amplifiers, to achieve a specified voltage gain or bandwidth;
1.4.6	Signal distortion	understand that the power supply requirements of an op-amp limit the output voltage swing; recognise clipping distortion, and describe how it can be reduced; recognise the distortion that occurs when the slew-rate of an op-amp is exceeded; select and use the formula for slew-rate: $SR = \frac{\Delta V_0}{\Delta t}$;

UNIT ET2 – Electronic Circuits and Components

AREA OF STUDY		***AMPLIFICATION***
		Candidates should be able to:
2.1	**Current, voltage, resistance and power**	recall and use $R = \frac{V}{I}$; apply Kirchhoff's laws; calculate the combined resistance of resistors connected in series and/or parallel; select appropriate values from the E24 series; perform calculations on voltage divider circuits ; define power as VI and apply the formula to calculate power dissipation;
2.2	**Timing circuits**	
2.2.1	RC networks	explain how capacitors can be used to form the basis of timing circuits; calculate the value of the time constant for an RC circuit using T = RC; sketch the charge and discharge curves for voltage and current; select and use the following formulae relating the voltage across a capacitor as a function of time: • $V_c = V_S (1 - e^{-t/RC})$ for a charging capacitor • $V_c = V_S e^{-t/RC}$ for a discharging capacitor; realise that • $V_C = 0.5\, V_S$ after $0.69\,RC$ • $V_C \approx V_S$ after $5\,RC$ for charging capacitors • $V_C \approx 0$ after $5\,RC$ for discharging capacitors;
2.2.2	Monostable circuits	recall that a monostable circuit has one stable state and one unstable state; describe how an inverter can be used with an RC network to form a simple time delay circuit; draw the circuit diagram for a monostable using a 555 timer IC and calculate the time period using T = 1.1 RC;
2.2.3	Astable circuits	recall that an astable circuit has two unstable states; explain the operation of a circuit based on a Schmitt inverter and estimate the operating frequency using $f \approx 1/RC$; draw the circuit diagram for an astable using a 555 timer IC; select and use formulae for • the time the output is high: $t_H = 0{\cdot}7\,(R_A+R_B)C$ • the time the output is low: $t_L = 0{\cdot}7R_BC$ • the frequency: $f = \frac{1}{0{\cdot}7(R_A + 2R_B)C}$ calculate the mark space ratio;

2.3 Semiconductor diodes

2.3.1	Silicon diodes	realise that the forward voltage is approximately 0.7 V when the diode is conducting;
2.3.2	Zener diodes	sketch current-voltage graphs for zener diodes, indicating the zener voltage V_Z and holding current $I_{Z\,(MIN)}$; select appropriate zener diodes given data on zener voltage and power rating;
2.3.3	Light emitting diodes	calculate series resistor values for DC LED indicator circuits; explain how an inverse parallel diode is used to protect the LED when used on an AC supply; estimate series resistor values for AC LED indicator circuits;

2.4 Simple power supplies

2.4.1	RMS	apply the formula $V_o = V_{rms}\sqrt{2}$ for a sinusoidal AC voltage;
2.4.2	Rectification	draw and understand the use of diodes in half-wave and full-wave bridge rectifiers; calculate the peak value of the output voltage of half-wave and full-wave rectifiers given the rms input voltage;
2.4.3	Capacitive smoothing	describe, by drawing a graph, the effect of a capacitor on the output waveform from a rectifier; know that the size of the ripple voltage is dependent on the method of rectification, the values of capacitance and load resistance; describe, by drawing graphs, the effect of loading on the output waveform of a smoothed rectifier;
2.4.4	Voltage regulation	describe how a zener diode can be used with a current limiting resistor to form a simple regulated voltage supply; calculate suitable values for limiting resistors and the maximum value of current available from the voltage supply; describe, by drawing a graph, the effect of loading on the output voltage of a regulated supply;

2.5	**Signal sources**	describe the use of photo transistors, light dependent resistors and ntc thermistors in voltage dividing chains to provide analogue signals; sketch and interpret response curves for the light dependent resistors and thermistor; calculate suitable values for resistors for use with the above devices; use Thevenin's theorem to draw equivalent circuits and predict the effect of loading; appreciate that the current through a potential divider should be at least 10 times that drawn by the output; explain how a Schmitt inverter can be used to provide signal conditioning with analogue signal sources and to eliminate mechanical switch bounce;
2.6	**Switching circuits**	
2.6.1	Voltage comparator	recall that the output state depends on the relative value of the two input states; design comparator switching circuits based on an op-amp;
2.6.2	npn transistors	describe the switching action of an npn transistor by making reference to its voltage transfer characteristic; perform calculations using $I_C = h_{FE} I_B$; know that V_{BE} depends on I_B and is approximately 0.7 V when the transistor is conducting; perform calculations on transistor switching circuits; estimate the value of h_{FE} from data provided; describe how a transistor switch can increase the output current capability of a comparator circuit;
2.6.3	Enhancement mode n channel MOSFETs	describe the switching action of n channel MOSFETs; recognise that MOSFETs have a very high input resistance; perform calculations using $I_D = g_M V_{GS}$; understand that r_{DS} decreases from a very high value to a very low value as V_{GS} is increased and is at a minimum value of r_{DSon} at saturation; perform calculations on MOSFET switching circuits; compare the performance of MOSFET and transistor switches;
2.6.4	Interfacing outputs	select suitable comparators, transistors and MOSFETs for connecting to signal sources and driving outputs such as lamps, buzzers, loudspeakers, motors, solenoids and relays; state the need for diode protection for comparators, transistors and MOSFETs;

UNIT ET3 – Programmable Control Systems Project

Introduction

*This unit focuses first on programming in a high level language using **ladder logic** programming, since this is prevalent in industrial control. However, many control systems, particularly in domestic systems such television remote control, car remote keys and heating controllers make use of micro-controllers such as the PIC-chip. Programming these controllers in **assembly language** will open the door to many powerful applications and exciting project work, whilst reinforcing the links with previous course units. This emphasis on project work is reflected in the method used to assess this unit. Further guidance on management and rationale appears in the section describing coursework in Section 6.5.1.*

AREA OF STUDY		***AMPLIFICATION***
		Candidates should be able to:
3.1	**Control Principles**	relate a design problem to the number and nature of inputs and outputs needed by a control system; apply a structured approach to programming control systems;
3.2	**Ladder Logic**	
3.2.1	Program design	design and test ladder logic programs which react to information from sensors to control outputs; design and test ladder logic programs which produce a sequence of events at the outputs which depends on the combination of inputs;
3.2.2	Ladder functions	build programs which: • incorporate analogue and digital inputs • count events • use time delays • produce a sequence of events • monitor inputs and take decisions • incorporate program tools, such as switches/software switches, in combinations which perform AND, OR and latching functions;
3.3	**Microcontrollers**	
3.3.1	Program design	design and test assembly language programs which react to information from sensors to control outputs; design and test assembly language programs which produce a sequence of events at the outputs which depends on the combination of inputs; synthesise programs using a range of standard sub-routines;

AREA OF STUDY		AMPLIFICATION
		Candidates should be able to:
3.3.2	Programming	build assembly language programs which: • incorporate digital inputs, • count events • use a time delay • produce a sequence of events • test bits to monitor inputs, and take decisions • use logic operations;
3.4	**Documentation**	provide for each program: • a description of the design problem, • a specification for the proposed solution, • a listing of the program, • a description of how the program works.

A Level

UNIT ET4 – Electronic Communications Systems

AREA OF STUDY	AMPLIFICATION
	Candidates should be able to:
4.1 Introduction	recall that communication is the transfer of meaningful information from one location to another; understand the following terms applied to communications systems: • analogue and digital signals • transmission medium • carrier • encoding / decoding • modulation / demodulation • gain / attenuation • base (signal) bandwidth • broadcast bandwidth • noise / distortion • multiplexer / demultiplexer • time division multiplexing • frequency division multiplexing • error detection, error correction recall and explain the relationship between bandwidth, data rate and the capacity to carry information.
4.2 Filters	
4.2.1 Introduction to filters	know and recall that the audio frequency range is approximately 20 Hz to 20 kHz; recall that high quality music transmission requires the full audio range; recall that the tonal quality of the received signal depends on the channel bandwidth allocated to it within the transmission system; recall that recognisable speech can be transmitted using a limited 300 Hz – 3 kHz range to reduce the bandwidth requirement; understand that a complex wave is constructed from a fundamental frequency plus a number of harmonic frequencies; draw the frequency spectrum of a sine wave and a square wave (qualitatively) before and after passing through an ideal filter with a given frequency spectrum.

AREA OF STUDY	**AMPLIFICATION**
	Candidates should be able to:
4.2.2 Passive RC filters	recognise, analyse and sketch characteristics for a low pass and high pass filter; design circuits to act as low pass or high pass filters; select and use the formula $X_C = \frac{1}{2\pi fC}$; understand the significance of the term impedance, and that it is a function of X_c and R in an R - C circuit; select and use the formula $Z = \sqrt{R^2 + X_C^2}$ to calculate the impedance of a series RC circuit. define and calculate the break frequency, selecting and using the formula $f_b = \frac{1}{2\pi RC}$ plot and interpret graphs showing the frequency response of an RC filter.
4.2.3 Resonant filters	recognise and sketch characteristics for a simple band pass filter draw the circuit diagram for a band pass filter based on a parallel LC circuit select and use the formula $X_L = 2\pi fL$; recall that resonance occurs in a parallel LC network when $X_C = X_L$ and hence calculate the resonant frequency; select and use the formula $f_0 \approx \frac{1}{2\pi\sqrt{LC}}$ where f_0 is the resonant frequency; appreciate that in practical inductors their resistance r_L, has the effect of lowering the value of f_0; select and use the formula for dynamic resistance, R_D, to calculate the output voltage of an unloaded filter at resonance where $R_D = \frac{L}{r_L C}$; know that the Q-Factor is a measure of the selectivity of the band pass filter; be able to calculate the Q-Factor, either from the frequency response graph, or component values; select and use the formulae: $Q = \frac{2\pi f_0 L}{r_L}$ and $Q = \frac{f_0}{\text{bandwidth}}$ for an unloaded circuit;

AREA OF STUDY	**AMPLIFICATION**
	Candidates should be able to:
4.3 Modulation techniques	
4.3.1 Data transfer	recall that the transfer of data can be carried out through free space and cable systems;
4.3.2 Amplitude Modulation	sketch and recognise the resulting waveforms for a sinusoidal carrier being amplitude modulated by a single frequency audio signal; draw and analyse graphs to show the resulting waveform, and frequency spectrum for a sinusoidal carrier amplitude modulated by an audio signal, to a given depth of modulation, m; select and use the formula: $m = \frac{(V_{max} - V_{min})}{(V_{max} + V_{min})} \times 100\%$, to calculate the depth of modulation for a given RF signal.
4.3.3 Frequency Modulation	sketch, recognise and analyse the resulting waveforms for a sinusoidal carrier being frequency modulated by a single frequency audio signal; recall that an FM-modulated carrier produces an infinite number of sidebands recall that the frequency deviation Δf_c is the maximum change in frequency of the carrier from its base value f_c . recall that the modulation index β is the FM equivalent to the depth of modulation; use the formula $\beta = \frac{\Delta f_c}{f_i}$, where f_i is the maximum frequency of the modulation signal ; appreciate that almost all the power of a transmitted FM signal is contained within a bandwidth of $2(1 + \beta) f_i$, where f_i is the maximum frequency of the modulating signal; recognise the frequency spectrum diagram for a sinusoidal carrier being frequency modulated by a single frequency audio signal for $\beta<1$, $\beta=1$, and $\beta=3$;
4.3.4 Comparison of AM and FM	compare the merits of AM and FM;
4.3.5 Pulse modulation	analyse and draw graphs to illustrate the following pulse carrier modulation techniques: • pulse width modulation • pulse position modulation • pulse amplitude modulation; analyse and draw graphs to illustrate the use of FSK to transmit digital data on an analogue carrier; analyse and draw graphs to illustrate phase shift keying.

AREA OF STUDY		AMPLIFICATION
		Candidates should be able to:
4.4	**AM radio receiver**	
4.4.1	Simple AM receiver	draw a block diagram, and circuit diagram for a simple radio receiver, consisting of antenna, tuned circuit, detector/demodulator, and earphones; describe the function of each of these sub-systems; appreciate that a tuned circuit is a variable frequency band pass filter; design a tuned circuit to select a particular carrier frequency; select and use the equation $C = \frac{1}{4\pi^2 f_0^2 L}$ to calculate the value of C to provide a given resonant frequency; use the frequency response curves of a loaded tuned circuit to explain poor selectivity;
4.4.2	Advanced radio receivers	explain that an RF amplifier can be used to improve sensitivity; explain that a superheterodyne receiver offers improved selectivity and sensitivity; draw a block diagram of a superheterodyne receiver, consisting of antenna, tuned RF amplifier, mixer, local oscillator, IF filter, IF amplifier, detector/demodulator, audio amplifier and loudspeaker; appreciate that the IF filter is a preset band pass filter; describe the function of each of these sub-systems;
4.5	**Digital Communications Systems**	
4.5.1	Introduction	compare analogue and digital communication in terms of noise, attenuation and distortion; state the function of Analogue to Digital converters (ADC) and Digital to Analogue converters (DAC);
4.5.2	Regeneration	recall and describe the difference between noise and distortion. understand that the signal to noise ratio degrades down a transmission line, and that regeneration restores the original signal; recognise, analyse and design inverting and non-inverting Schmitt trigger circuits to regenerate digital signals;
4.5.3	Shift Registers	recognise, analyse and design circuits containing D-type flip-flops to form parallel-in serial-out (PISO) registers and serial-in-parallel-out (SIPO) registers; draw timing diagrams.

AREA OF STUDY	AMPLIFICATION
	Candidates should be able to:
4.5.4 Pulse code modulation (PCM)	analyse and draw graphs to illustrate pulse amplitude modulation (PAM) techniques; relate required sampling frequency to the highest frequency in the signal; draw a block diagram for, and describe the operation of, a PCM communication system consisting of: transmitter, • low pass filter • sampling gate • sampling clock • ADC • PISO shift register • PISO clock and receiver, • Schmitt trigger • SIPO shift register • SIPO clock • DAC • low pass filter; relate resolution to the number of sampling levels, and select and use the formula: resolution = input voltage range / 2^n; describe how time division multiplexing (TDM) can be used to improve the capacity of a PCM communications link; use given data to calculate how many channels can be incorporated into a PCM communications link, using TDM;
4.5.5 Asynchronous transmission	describe asynchronous character framing in terms of the start and stop bits, data bits and parity bit; appreciate that the ability to detect and correct errors that occur during digital transmissions is not possible with analogue systems; describe how using extra parity bits can provide error detection and correction; describe and use two-bit parity-bit systems to speed up data transfer by only having to retransmit half of the data when an error is detected describe and use a five parity-bit system to identify and correct a single error if it has occurred; realise that even with multiple parity-bit systems it is not always possible to detect and correct errors when more than one bit is affected; appreciate that there is a trade off between the ability to check and correct data and the extra transmission costs; realise that in very noisy or sensitive applications it is often essential to have a high level of data checking despite the extra cost involved.

UNIT ET5 – Electronic Systems Applications

AREA OF STUDY	AMPLIFICATION
	Candidates should be able to:
5.1 Counting Systems	
This section contrasts the performance of ripple counters, covered in ET1, with synchronous counters, based on D-type flip-flops, another component of ET1. It also includes the use of synchronous counters as sequence generators.	
5.1.1 Ripple counters	describe the effect of propagation delay on count rate;
5.1.2 Synchronous counters	draw a block diagram showing how D-type flip-flops can be connected to form a synchronous counter to meet a given specification; explain how simultaneous clocking of D-type flip-flops overcomes limitation of ripple counters at high counting speed; draw the state diagram for a synchronous counter given a system specification; explain the significance and cause of stuck states, and describe how they can be avoided by directing unused states back into the main sequence; manipulate unused (don't care) states to produce simpler solutions; analyse and design a synchronous counter (up to 3 bits) to obtain the state diagram for the sequence it produces;
5.2 Microcontroller Systems *Microcontrollers were the subject of part of ET3. They appear in a wide variety of everyday devices. This section gives an overview of their architecture, and looks at techniques for converting signals between analogue and digital format, for microcontroller and other electronic systems. This develops the work done in ET1 on voltage amplifiers and in ET2 on comparators. The work on microcontrollers will focus on the PIC 16F84 microcontroller.*	

AREA OF STUDY	**AMPLIFICATION**
	Candidates should be able to:
5.2.1 PIC 16Cxx microcontrollers	recall the architecture of a PIC microcontroller, consisting of CPU, clock, data memory, program memory and input/output ports, connected by buses; explain, and give examples of, the use of interrupts to allow an external device to be serviced on request; draw a circuit diagram to show how an external device can be connected to a PIC microcontroller to cause an interrupt; use a vector address to point to an interrupt service routine; write and analyse given code to configure the ports as input or output ports, using the file registers called TRISA and TRISB; configure the INTCON file register to enable an external interrupt; recognise the need to protect the contents of the working register when writing an interrupt service routine; devise and analyse code using the following instructions: bcf, bsf, btfss, call, clrf, goto, movf, movlw, movwf, retfie; incorporate given subroutines into program code;
5.2.2. Digital to Analogue Converters (DAC)	analyse and design a DAC based on an op-amp summing amplifier to meet a given specification;
5.2.3 Analogue to Digital Converters (ADC)	analyse and design a flash converter based on comparators to meet a given specification; recall the factors affecting the resolution of a flash converter; calculate the resolution of a n-bit flash converter using the formula: *resolution = input voltage range / 2^n;* analyse and design a priority encoder to meet a given specification;

5.3 Power Supply Systems

This section develops the work done on simple power supplies in ET2. Specifically, it adds an emitter follower stage, and a non-inverting voltage amplifier, covered in ET1, to improve line and load regulation.

5.3.1 Load and Line regulation	explain what is meant by the terms load regulation and line regulation;
5.3.2 Emitter Follower	draw the circuit diagram for an emitter follower based on an npn transistor; recall that the input impedance ~ h_{FE} R_E and that $V_{OUT} = V_{IN} - 0.7$ V;

AREA OF STUDY	**AMPLIFICATION**
	Candidates should be able to:
5.3.3 Voltage Regulator	design and analyse a voltage regulator based on a zener diode, an emitter follower and a non-inverting amplifier; select and use the gain formula $V_L \approx V_Z\left(1+\frac{R_F}{R_1}\right)$ to calculate output voltage;

5.4 Instrumentation Systems

In an instrumentation system the signals from one or more sensors are processed by instrumentation amplifiers and the results are displayed on a data presentation device, such as a centre-zero analogue meter, a bar graph display or a LCD display. This section focuses on the sensor sub-systems, developing the work done on simple voltage divider sub-systems in ET2, and on the instrumentation amplifier.

5.4.1 Sensors	describe the use of the following analogue sensors: thermistors and strain gauges, describe the use of the following digital sensors: slotted discs (for sensing rotational speed), encoded discs (for sensing angular position); recall the Gray code (3 bit) and explain its use in encoded discs;
5.4.2 Sensor sub-systems	analyse and design sensor sub-systems which incorporate thermistors and strain gauges in bridge circuits; recall the advantages of a bridge circuit compared to a simple voltage divider circuit;
5.4.3 Instrumentation amplifier	recall, and explain the significance of, the ideal properties of an instrumentation amplifier – high input impedance and high common-mode rejection ratio; analyse and design instrumentation amplifiers based on the op-amp difference amplifier circuit; select and use the formula: $V_{OUT} = V_{DIFF}\left(\frac{R_F}{R_1}\right)$;
5.4.4 Digital Processing	design a logic system to process the output of slotted and encoded discs, to meet a given specification;

5.5 High Power Switching Systems

Industrial operations such as lighting, heating, electric welding and motor speed control require the delivery of a variable and controlled amount of electrical power. Use of variable resistors is expensive and wasteful of energy. The thyristor is small, inexpensive and wastes little energy. In industry, it can control currents of several hundred amps at high voltage. This section gives an introduction to the behaviour of this device

AREA OF STUDY	**AMPLIFICATION**
	Candidates should be able to:
5.5.1 General thyristor characteristics	recall the conditions under which a thyristor conducts; explain the significance of the following terms: holding current, minimum gate voltage, minimum gate current.;
5.5.2 DC switching circuit	describe the advantages of using a thyristor to switch a high power load, compared to using a transistor or a relay; explain the process of capacitor commutation to switch off a thyristor; use given data to design a DC thyristor switching circuit;
5.5.3 AC switching circuit	draw the circuit diagram for a phase control circuit, using a RC network and a diac; draw and analyse graphs that show the phase difference between supply voltage and capacitor voltage in RC circuits; sketch voltage/time graphs for the waveforms across the capacitor, thyristor and load in a phase control circuit; select and use the formula $\phi = \tan^{-1}\left(\frac{R}{X_C}\right)$ to calculate the phase shift between supply voltage and capacitor voltage

5.6 Audio Systems

This section develops the work on voltage amplifiers in ET1 to look at public address systems, consisting of input sources, pre-amplifiers, mixer, tone controls, power amplifier and loudspeaker. The work done on passive filters in ET4 is extended to include active filters used as tone controls.

5.6.1 Pre-amplifiers	recall the conditions required for maximum voltage transfer between sub-systems; analyse a unity gain op-amp voltage follower, used for impedance matching; analyse and design a multi-stage voltage amplifier, incorporating decoupling capacitors, to provide a specified bandwidth and voltage gain;
5.6.2 Mixer	analyse and design a mixer circuit based on a summing amplifier select and use the formula: $V_{OUT} = -R_F\left(\frac{V_1}{R_1} + \frac{V_2}{R_2} + \frac{V_3}{R_3}\right)$;

AREA OF STUDY	**AMPLIFICATION**
	Candidates should be able to:
5.6.3 Tone controls	define the break frequency for a filter; select and use the formula: $f_b = \frac{1}{2\pi RC}$ to calculate break frequency; draw and interpret log gain / log frequency graphs for filters; analyse and design the following first order active filter circuits based on an op-amp inverting amplifier: ▪ bass boost, ▪ treble boost, ▪ bass cut ▪ treble cut;
5.6.4 Audio power amplifiers	recall and apply the maximum power transfer theorem; recall that an emitter follower can be used as a simple power amplifier, with the benefit of high input impedance and low output impedance; draw the circuit diagram for an emitter follower: ▪ using resistor bias; ▪ using a dual rail power supply; analyse and sketch graphs of the waveforms in an emitter follower power amplifier; draw circuit diagram for, and sketch graphs of the waveforms in a push-pull power amplifier, consisting of a npn and pnp emitter follower; explain what is meant by crossover distortion, and describe how it can be eliminated; select and use the formula: $P_{MAX} = \frac{V_S^{\,2}}{8R_L}$ [where V_S is the rail-to-rail voltage] to calculate the maximum power dissipated in the load of a push-pull power amplifier;

UNIT ET6 – Electronic Design Project

Introduction

The project undertaken should be such that it can be completed in approximately 25 hours. Candidates should be encouraged to select projects in which they are interested and which are neither under nor over ambitious. The overall system should be developed as a number of sub-systems which should be individually tested and evaluated before being incorporated into the complete system. This will ensure that the complete system grows by a gradual and incremental process, having been assessed at each stage of its development

AREA OF STUDY		***AMPLIFICATION***
		Candidates should be able to:
6.1	**Project planning**	write a detailed specification for a solution to the problem, using appropriate technical terminology; research sources of information and justify its relevance; draw a labelled block diagram and describe the function of each block, for the proposed solution;
6.2	**System development**	develop the chosen solution as a series of sub-systems and for each sub-system: write a specification to define the desired performance of the sub-system; consider, where possible, alternative circuits which meet the sub-system specification, giving reasons for selecting the preferred circuit; give a circuit diagram; select/calculate component values; devise procedures to test the circuit ; evaluate its performance against the sub-system specification; modify the circuit, where necessary, to meet the specification; apply appropriate safety procedures as set out in the following publications: IET Wiring Regulations-Requirements for Electrical Installation BS 7671: 2001, *HSE-Management of Health and Safety at work: Approved Code of Practice*.
6.3	**Complete system**	plan an organised layout for the complete system on either prototype board, strip-board or printed circuit board; devise procedures to test the complete system in terms of the parameters given in the system specification; evaluate its performance against that system specification; produce a set of recommendations for further development;
6.4	**Documentation**	write a detailed report on the development of the project, including a photograph of the complete system;

5 SCHEME OF ASSESSMENT

AS and A level qualifications are available to candidates following this specification.

AS

The AS is the first half of an A level course. It will contribute 50% of the total A level marks. Candidates must complete the following **two units** in order to gain an AS qualification.

		Weighting Within AS	Weighting Within A level
ET1	Introduction to Digital & Analogue Systems	35%	17.5%
ET2	Electronic Circuits & Components	35%	17.5%
ET3	Programmable Control Systems Project	30%	15%

ET1: Written Paper (1¼ hours)

The paper will consist of approximately 8 questions with a raw mark total of 60. There will be no sections. All questions will be compulsory.

ET2 : Written Paper (1¼ hours)

The paper will consist of approximately 8 questions with a raw mark total of 60. There will be no sections. All questions will be compulsory.

ET3: Internal Assessment

For ET3, candidates will be expected to submit no more than two programming mini-projects reports for each of the two levels of programming. The marking criteria for this unit are listed in the Coursework Mark Booklet (See Appendix 1).

A Level

The A level specification consists of two parts: Part 1 (AS) and Part 2 (A2).

Part 1 (AS) may be taken separately and added to A2 at a further examination sitting to achieve an A level qualification, or alternatively, both the AS and A2 may be taken at the same sitting.

Candidates must complete the AS units outlined above plus a further two units to complete A level Electronics. The A2 units will contribute 50% of the total A level marks.

		Weighting within A2	Weighting within A level
ET4*	Electronic Communications Systems	30%	15%
ET5*	Electronic Systems Applications	40%	20%
ET6*	Electronic Design Project	30%	15%

*Includes synoptic assessment

ET4: Written Paper (1 hour)

The paper will consist of approximately 7 questions with a raw mark total of 50. There will be no sections. All questions will be compulsory.

ET5 : Written Paper (1½ hours)

The paper will consist of approximately 9 questions with a raw mark total of 70. There will be no sections. All questions will be compulsory.

ET6: Internal Assessment

For ET6, candidates will be expected to submit a project report. The marking criteria for this unit are listed in the Coursework Mark Booklet (See Appendix 2).

Synoptic Assessment

Synoptic assessment, testing candidates' understanding of the connections between the different elements of the subject and their holistic understanding of the subject, is a requirement of all A level specifications. In the context of Electronics this means:

ET4: The logic and circuit aspects of the content of this unit build upon the knowledge and skills acquired in ET1 and ET2. Questions will, as appropriate examine these areas.

ET5: This is a fundamentally synoptic unit. All areas build upon the knowledge and skills acquired in units ET1, 2, 3 and 4. This is expanded upon in the italicised statement at the beginning of each section of ET5. Questions will examine these connections and cross-links between them.

ET6: This internally-assessed unit requires candidates to apply skills and understanding they have acquired throughout the course to the solution of a practical problem.

Quality of Written Communication

Candidates will be required to demonstrate their competence in written communication in all assessment units where they are required to produce extended written material: In GCE Electronics this requirement is found in units ET3 and ET6. Mark schemes for these units include the following specific criteria for the assessment of written communication.

- legibility of text; accuracy of spelling, punctuation and grammar; clarity of meaning;
- selection of a form and style of writing appropriate to purpose and to complexity of subject matter;
- organisation of information clearly and coherently; use of specialist vocabulary where appropriate.

In ET3 the quality of a candidate's written communication is addressed in the assessment criteria in Section 4 of both part A and part B [See appendix 1]. In ET6 it is addressed in section 8 [See appendix 2].

Availability of Units

See the table on page 2 of this specification for details of when the units are available.

Awarding, Reporting and Re-sitting

The overall grades for the GCE AS qualification will be recorded as a grade on a scale from A to E. The overall grades for the GCE A level qualification will be recorded on a grade scale from A* to E. Results not attaining the minimum standard for the award of a grade will be reported as U (Unclassified). Individual unit results and the overall subject award will be expressed as a uniform mark on a scale common to all GCE qualifications (see table below). The grade equivalence will be reported as a lower case letter ((a) to (e)) on results slips, but not on certificates:

	Max. UMS	A	B	C	D	E
ET1 and 2 (weighting 17.5%)	105	84	74	63	53	42
ET3, 4 and 6 (weighting 15 %)	90	72	63	54	45	36
ET5 (weighting 20%)	120	96	84	72	60	48
AS Qualification	300	240	210	180	150	120
A Qualification	600	480	420	360	300	240

At A level, Grade A* will be awarded to candidates who have achieved a Grade A in the overall A level qualification and 90% of the total uniform marks for the A2 units.

Candidates may re-sit units prior to certification for the qualification, with the best of the results achieved contributing to the qualification. Individual unit results, prior to certification of the qualification have a shelf-life limited only by the shelf-life of the specification.

6 *KEY SKILLS*

Key Skills are integral to the study of AS/A level Electronics and may be assessed through the course content and the related scheme of assessment as defined in the specification. The following key skills can be developed through this specification at level 3:

- Communication
- Application of Number
- Problem Solving
- Information and Communication Technology
- Working with Others
- Improving Own Learning and Performance

Mapping of opportunities for the development of these skills against Key Skills evidence requirement is provided in 'Exemplification of Key Skills for Electronics, available on the WJEC website.

7 PERFORMANCE DESCRIPTIONS

Introduction

Performance descriptions have been created for all GCE subjects. They describe the learning outcomes and levels of attainment likely to be demonstrated by a representative candidate performing at the A/B and E/U boundaries for AS and A2.

In practice most candidates will show uneven profiles across the attainments listed, with strengths in some areas compensating in the award process for weaknesses or omissions elsewhere. Performance descriptions illustrate expectations at the A/B and E/U boundaries of the AS and A2 as a whole; they have not been written at unit level.

Grade A/B and E/U boundaries should be set using professional judgement. The judgement should reflect the quality of candidates' work, informed by the available technical and statistical evidence. Performance descriptions are designed to assist examiners in exercising their professional judgement. They should be interpreted and applied in the context of individual specifications and their associated units. However, performance descriptions are not designed to define the content of specifications and units.

The requirement for all AS and A level specifications to assess candidates' quality of written communication will be met through one or more of the assessment objectives.

The performance descriptions have been produced by the regulatory authorities in collaboration with the awarding bodies.

AS performance descriptions for electronics

	Assessment objective 1	**Assessment objective 2**	**Assessment objective 3**
Assessment objectives	**Knowledge and understanding of science and of How science works** Candidates should be able to: • recognise, recall and show understanding of scientific knowledge • select, organise and communicate relevant information in a variety of forms.	**Application of knowledge and understanding of science and of How science works** Candidates should be able to: • analyse and evaluate scientific knowledge and processes • apply scientific knowledge and processes to unfamiliar situations including those related to issues • assess the validity, reliability and credibility of scientific information.	**How science works** Candidates should be able to: • demonstrate and describe ethical, safe and skilful practical techniques and processes, selecting appropriate qualitative and quantitative methods • make, record and communicate reliable and valid observations and measurements with appropriate precision and accuracy • analyse, interpret, explain and evaluate the methodology, results and impact of their own and others' experimental and investigative activities in a variety of ways.
A/B boundary performance descriptions	Candidates characteristically: a) demonstrate knowledge and understanding of most principles, concepts and facts from the AS specification b) select relevant information from the AS specification c) organise and present information clearly in appropriate forms using scientific terminology.	Candidates characteristically: a) apply principles and concepts in familiar and new contexts involving only a few steps in the argument b) describe significant trends and patterns shown by data presented in tabular or graphical form c) interpret and explain phenomena with few errors and present arguments and evaluations clearly d) carry out structured calculations with few errors e) design a system to perform a stated function for most situations within the context of the AS specification.	Candidates characteristically: a) devise and plan experimental and investigative activities, selecting appropriate techniques b) demonstrate safe and skilful practical techniques c) make observations and measurements with appropriate precision and record these methodically d) interpret, explain, evaluate and communicate the results of their own and others' experimental and investigative activities, in appropriate contexts.
E/U boundary performance descriptions	Candidates characteristically: a) demonstrate knowledge and understanding of some principles and facts from the AS specification b) select some relevant information from the AS specification c) present information using basic terminology from the AS specification.	Candidates characteristically: a) apply a given principle to material presented in familiar or closely related contexts involving only a few steps in the argument b) describe some trends or patterns shown by data presented in tabular or graphical form c) provide basic explanations and interpretations of some phenomena, presenting very limited evaluations d) carry out some steps within calculations e) design a simple system to perform a stated function for some situations within the context of the AS specification.	Candidates characteristically: a) devise and plan some aspects of experimental and investigative activities b) demonstrate safe practical techniques c) make observations and measurements and record them d) interpret, explain and communicate some of the results of their own and others' experimental and investigative activities, in appropriate contexts.

A2 performance descriptions for electronics

	Assessment objective 1	**Assessment objective 2**	**Assessment objective 3**
Assessment objectives	**Knowledge and understanding of science and of How science works** Candidates should be able to: • recognise, recall and show understanding of scientific knowledge • select, organise and communicate relevant information in a variety of forms.	**Application of knowledge and understanding of science and of How science works** Candidates should be able to: • analyse and evaluate scientific knowledge and processes • apply scientific knowledge and processes to unfamiliar situations including those related to issues • assess the validity, reliability and credibility of scientific information.	**How science works** Candidates should be able to: • demonstrate and describe ethical, safe and skilful practical techniques and processes, selecting appropriate qualitative and quantitative methods • make, record and communicate reliable and valid observations and measurements with appropriate precision and accuracy • analyse, interpret, explain and evaluate the methodology, results and impact of their own and others' experimental and investigative activities in a variety of ways.
A/B boundary performance descriptions	Candidates characteristically: a) demonstrate detailed knowledge and understanding of most principles, concepts and facts from the A2 specification b) select relevant information from the A2 specification c) organise and present information clearly in appropriate forms using scientific terminology.	Candidates characteristically: a) apply principles and concepts in familiar and new contexts involving several steps in the argument b) describe significant trends and patterns shown by complex data presented in tabular or graphical form c) interpret and explain phenomena effectively, presenting arguments and evaluations clearly and logically d) carry out extended calculations, with little or no guidance e) design a system to perform a stated function for most situations in the context of the A2 specification f) select a wide range of facts, principles and concepts from both AS and A2 specifications g) link together appropriate facts, principles and concepts from different areas of the specification.	Candidates characteristically: a) devise and plan experimental and investigative activities, selecting appropriate techniques b) demonstrate safe and skilful practical techniques c) make observations and measurements with appropriate precision and record these methodically d) interpret, explain, evaluate and communicate the results of their own and others' experimental and investigative activities, in appropriate contexts.
E/U boundary performance descriptions	Candidates characteristically: a) demonstrate knowledge and understanding of some principles and facts from the A2 specification b) select some relevant information from the A2 specification c) present information using basic terminology from the A2 specification.	Candidates characteristically: a) apply given principles or concepts in familiar and new contexts involving a few steps in the argument b) describe, and provide a limited explanation of, trends or patterns shown by complex data presented in tabular or graphical form c) provide basic explanations and interpretations of some phenomena, presenting very limited arguments and evaluations d) carry out routine calculations, with guidance e) design a simple system to perform a stated function for some situations within the context of the A2 specification f) select some facts, principles and concepts from both AS and A2 specifications g) put together some facts, principles and concepts from different areas of the specification.	Candidates characteristically: a) devise and plan some aspects of experimental and investigative activities b) demonstrate safe practical techniques c) make observations and measurements and record them d) interpret, explain and communicate some of the results of their own and others' experimental and investigative activities, in appropriate contexts.

8 GUIDANCE ON THE MANAGEMENT OF INTERNAL ASSESSMENT

8.1 Unit ET3 is intended to introduce candidates to two software control techniques. The first uses ladder logic, which is a high-level language, widely used in industrial control systems. The other uses assembly language which is widely used to program microcontrollers used for consumer products. In neither case is it expected that students will be exposed to an exhaustively detailed course, but rather that they will acquire enough skill to construct simple programs to carry out control tasks.

Ladder logic should be introduced using a graphics interface such as 'ICON' or 'MEDOC'. In this way, candidates can quickly learn the action of, and how to program, the functions listed in the Unit specification. The graphics interface allows candidates to link these functions together to synthesise simple control systems and to test them 'on-screen'. It is not expected that candidates construct any external circuitry to test their programs. The assessment looks at the candidates' ability to incorporate a number of these functions into a program in an appropriate and sensible way. The mark gained depends partly on how many functions are successfully integrated into a program. The candidate can submit up to two separate programs, to make it easier to cover the range of functions, and to make the assessment more accessible to a wide ability range.

In the second section of the unit, candidates will be introduced to a number of standard subroutines that make the PIC microcontroller carry out functions similar to those studied in the ladder logic section by means of a template. Candidates should be able to incorporate these subroutines into a larger program. It is not expected that candidates be familiar with every instruction in the instruction set, or use every programming technique available. Several manufacturers produce PIC development systems which can be used to deliver this part of the unit. The treatment should not be limited to 'on-screen' design and emulation, but should involve the actual programming of a PIC chip, and its testing remotely on a development board. As with the assessment of the ladder logic section, the candidate submits a portfolio of up to two programs to cover the range of program commands specified.

For both ladder logic and PIC programming, the coursework submission must include, for each program, a description of the design problem, a specification for the proposed solution, a listing of the program, a description of how the program works and a comparison of the final performance against the initial specification.

The WJEC provides a project template for the PIC aspect of this unit, which gives a possible structure for the assembly language program. It is recommended that centres make use of this or a similar template.

8.2 The A2 coursework undertaken for unit ET6 should be such that it can be completed in 25 hours. Candidates should be encouraged to select projects in which they are interested and which are neither under nor over ambitious. Having decided on a design brief for the project, the candidate should undertake appropriate research so that a list of performance parameters (specification) can be given. It is expected that the specification will contain realistic numerical values against which the final performance of the work can be judged.

The overall system should be developed as a number of sub-systems which should be individually tested and evaluated before being incorporated into the complete system. This will ensure that the complete system grows by a gradual and incremental process, having been assessed at each stage of its development. Computer simulations may be used as a development tool in sub-system design.

For microcontroller-based projects a sub-routine can be considered a sub-system as long as a specification is provided for it and it can be tested and evaluated in a similar fashion to a component-based sub-system. To meet the assessment requirements a microcontroller-based project will also need to include, as a minimum, some component-based processing sub-systems for the input/output signals of the microcontroller (in addition to the microcontroller circuitry).

Construction of the system may be on prototype board, strip board or printed circuit board. The unit specification does not require candidates to 'hard wire' their system. Whichever method of construction is chosen the layout and mounting of components and wiring should be neat and logical, assisting the design, testing and fault finding of the system.

The system should be fully tested when the project is complete. The testing should be documented with results being displayed in tables and graphs, where appropriate. These tests will enable the candidate to assess the system and identify faults and limitations. The candidate should attempt to modify the system to correct for any limitations and then produce a final set of performance figures for the completed system. The candidate should then evaluate the final system against the initial specification and suggest further developments.

The candidate should fully document the development of the coursework project in a report. It is the evidence contained within this report upon which the coursework is marked and assessed. It should be presented in a logical order that is easy to read and understand. It should be free from repetition and should contain an acknowledgement of all sources of information and help.

The WJEC provides a project template which gives a possible structure for the report. It is recommended that centres make use of this template.

Further amplification is given in Unit ET6.

8.3 Supervision and Authentication of Coursework

Candidates are forbidden to indulge in any unfair practice whilst preparing coursework for assessment as part of the examination. Candidates must be informed of the WJEC regulations concerning malpractice. Any candidate suspected of using unfair means must be reported to the WJEC immediately. If the WJEC is satisfied that a breach of regulations has occurred, the candidate will be liable to disqualification from the whole of the current examination. Candidates will be required to certify that they have read and understood the regulations relating to unfair practice by signing a declaration on a coursework coversheet provided by the WJEC.

Sufficient supervision must be provided so that centres can give assurance that all possible means have been taken to ensure that the assessments submitted are the work of the candidates concerned. As much coursework as possible must be conducted under the direct supervision of teachers. The teacher responsible for the supervision of candidates' work will be required to certify that the marks submitted were awarded in accordance with the specification and that they are entirely satisfied that the work submitted is that of the candidate concerned.

8.4 The Marking of Coursework

Marks should be awarded for the criteria listed in the Coursework Mark Booklets (See Appendix 1 for Unit ET3 coursework and Appendix 2 for Unit ET6 coursework). Standards are set by the use of marking criteria which describe the performance expected for a particular mark. These criteria should be interpreted at the appropriate level, i.e. AS or A2. For example a response which may be deemed appropriate at GCSE might be considered too trivial at AS or A2 to attract credit. Exemplar projects are available from WJEC to illustrate the level of response required.

In most cases each of the assessment criteria covers a set of related features. Exemplification statements are given in the Mark Booklets which indicate the features which should be present for a candidate to be awarded full marks for that criterion.

Marks should only be awarded for work which is that of the candidate. It is permitted to give the candidate detailed guidance in one area to allow her/him to make progress. In such cases, no marks can be awarded for the input from the teacher, but subsequent work which is the candidate's own can be credited. In ET6, criterion 7(a) assesses additionally the degree to which the candidate has been guided.

Marks should only be awarded when there is supporting evidence. Supervisors must annotate each candidate's Coursework Mark Booklet and/or the relevant section of the work to identify the location of relevant evidence. Annotation should also be provided to indicate to what degree the final performance met the initial specification. Further guidance on annotation and awarding intermediate marks will be issued by WJEC.

For Unit ET6 each candidate's report must contain clear photographic evidence of the completed circuit. A Coursework Cover Sheet is provided as an integral part of the Coursework Mark Booklet.

The centre is responsible for carrying out internal standardisation where two or more teachers have been involved in the marking of the work submitted for a single unit.

8.5 Moderation of coursework

Moderation of the internal assessments will take place on the basis of a detailed scrutiny of the project documentation of all candidates by a WJEC appointed moderator. Each project report together with a completed Coursework Mark Booklet (and photographic evidence in the case of Unit ET6) must be sent to the moderator. A moderation visit may be made to the centre if this is considered to be necessary to complete the moderation process. Circumstances in which visits may be needed may be those where the work submitted is unclear, confusing, problematic or where a major adjustment of the centre's marks is indicated. Visits may also be made to centres to monitor samples of any hardware produced in projects. Advanced notice of such visits will be given by the WJEC.

Appendix 1: ET3 Internal Assessment Mark Booklet

WELSH JOINT EDUCATION COMMITTEE
GENERAL CERTIFICATE OF EDUCATION
A LEVEL

CYD-BWYLLGOR ADDYSG CYMRU
TYSTYSGRIF ADDYSG GYFFREDINOL
SAFON UWCH

Coursework Mark Booklet

GCE Electronics Unit ET3

Centre Name _____

Centre Number _____

Candidate's name (in full) _____

Candidate's ID number _____

NOTICE TO CANDIDATE

The work you submit for assessment must be your own.

If you copy from someone else, allow another candidate to copy from you, or if you cheat in any other way, you may be disqualified from at least the subject concerned.

Declaration by candidate

I have read and understood the **Notice to Candidate** (above). I have produced the attached work without assistance other than that which my teacher has explained is acceptable within the specification.

Candidate's signature: ……	**Date:** ……/2009

Declaration by teacher

I confirm that the candidate's work was conducted under the conditions laid out by the specification.

I have authenticated the candidate's work and am satisfied that to the best of my knowledge the work produced is solely that of the candidate.

Teacher's signature: ……	**Date**: ……/2009

Notes for supervisors:

- It is a requirement that supervisors annotate each candidate's Coursework Mark Booklet and/or the relevant section of the work to identify the location of relevant evidence.
- Annotation should also be provided to indicate to what degree the final performance met the initial specification

SECTION A Ladder Logic Programming

==========

1. Ladder programming functions:

To satisfy a design brief the Candidate has written a program which:		**LLP1**	**LLP2**
a	makes use of switches and sensors to perform AND **and** OR functions;[2]		
b	makes effective use of software switches to control output devices; [3] *Exemplification: To achieve all 3 marks a candidate could have used a software switch as a latch, triggered a software switch from an output on another rung, and combined software switches to control an action on a single rung.*		
c	uses, with justification, programming functions to count input events and to time and sequence appropriate output actions. [4] *Exemplification: To achieve all 4 marks a candidate could have used a counter, two types of timer function, a sequencer function and pulse production (justifying the frequency chosen)*		

2. Integration of techniques:

The Candidate has:

a	integrated an appropriate range of programming functions into the program. [2] E*xemplification: To achieve 2 marks a candidate should have used at least 7 different functions (as given in the exemplification in section 1).*		

3. Program performance:

The initial specification and final performance:

a	agree on relevant parameters (with evidence of appropriate testing). [3] *Exemplification: To achieve all 3 marks a candidate's program should perform in accordance with at least 4 parameters on the design brief and the documentation should give details of the testing used to compare the final performance with the specification.*		

4. Project documentation:

The Candidate has provided:

a	a design brief and specification; [3] *Exemplification: To achieve all 3 marks the candidate's specification should contain at least 4 parameters.*		
b	an explanation of the operation of the program. [3] *Exemplification: To achieve all 3 marks the candidate should describe the function of each individual rung and explain the structure of the program with a correct use of technical terms.*		

	Total Mark (maximum 20)	

SECTION B – Micro-Controller Programming

==========

1. Programming:

The Candidate has built an assembly language program that has:		**PP1**	**PP2**
a	configured inputs to use information from external events to produce appropriate output actions. [4] *Exemplification: To achieve 4 marks a candidate's program should configure the i/p and o/p terminals, generate a pre-determined sequence of output events, reacted to and used information from inputs to control outputs and counted external events.*		

The Candidate has:

b	used a range of commands which effectively handled data at a bit and file level; [3] *Exemplification: To achieve 3 marks a candidate should have moved data between registers, set bits, cleared bits/files and tested bits.*		
c	used branching commands effectively within a structured program; [2] *Exemplification: To achieve 2 marks a candidate should have used branched commands and called a subroutine.*		
d	used commands which effectively performed arithmetic and logical functions; [2]		
e	integrated effectively at least 4 different commands in one program. [1]		

2. Program performance:

The initial specification and final performance:

a	agree on relevant parameters (with evidence of appropriate testing). [3] *Exemplification: To achieve all 3 marks a candidate's program should perform in accordance with at least 4 parameters on the design brief and the documentation should give details of the testing used to compare the final performance with the specification.*		

3. Project documentation:

The Candidate has provided:

a	a design brief and specification; [3] *Exemplification: To achieve all 3 marks the candidate's specification should contain at least 4 parameters.*		
b	an annotated flowchart describing the operation of the program. [2]		

Total Mark (maximum 20)	

Guidance notes for Assessors:
The exemplification statements are intended to give an indication of the level of performance which will attract full marks. In most cases the exemplification covers a group of related but individual attributes. Intermediate performance can be credited for candidates who have fulfilled some of the requirements fully or partially met all/most of the requirements.

Appendix 2: ET6 Internal Assessment Mark Booklet

WELSH JOINT EDUCATION COMMITTEE
GENERAL CERTIFICATE OF EDUCATION
A LEVEL

CYD-BWYLLGOR ADDYSG CYMRU
TYSTYSGRIF ADDYSG GYFFREDINOL
SAFON UWCH

Coursework Mark Booklet

GCE Electronics Unit ET6

Centre Name _____

Centre Number _____

Candidate's name (in full) _____

Candidate's ID number _____

NOTICE TO CANDIDATE

The work you submit for assessment must be your own.

If you copy from someone else, allow another candidate to copy from you, or if you cheat in any other way, you may be disqualified from at least the subject concerned.

Declaration by candidate

I have read and understood the **Notice to Candidate** (above). I have produced the attached work without assistance other than that which my teacher has explained is acceptable within the specification.

Candidate's signature: ……	**Date:** ……/2010

Declaration by teacher

I confirm that the candidate's work was conducted under the conditions laid out by the specification.

I have authenticated the candidate's work and am satisfied that to the best of my knowledge the work produced is solely that of the candidate.

Teacher's signature: ……	**Date**: ……../2010

Notes for supervisors:

- It is a requirement that supervisors annotate each candidate's Coursework Mark Booklet and/or the relevant section of the work to identify the location of relevant evidence.
- Annotation should also be provided to indicate to what degree the final performance met the initial specification

1. Initial specification:

The Candidate has:		Mark	See report page(s)
a	given a qualitative and quantitative specification. [3] *Exemplification: In order to achieve 3 marks a candidate should have given a description of the problem together with a full quantitative and qualitative specification.*		

2. Project planning and research:

The Candidate has:

a	undertaken and communicated relevant research; [2]		
b	explained how the planned system works in terms of the function of its blocks. [3] *Exemplification: 1 mark may be achieved by a block diagram of the whole system.*		

3. Project development:

The Candidate has:

a	given specifications and detailed descriptions and circuit diagrams of subsystems and the complete system; [4] *Exemplification: In order to achieve 4 marks, the candidate should have given specifications and circuit diagrams for 5 or more sub-systems and a labelled circuit diagram for the whole system.*		
b	considered alternative sub-system designs and given reasons for the chosen designs; [4] *Exemplification: In order to achieve 4 marks a candidate should have considered alternative sub-system designs for at least 4 sub-systems and given comprehensive reasons for the final choice in each case.*		
c	described and given the results of numerical (or other relevant) test procedures for sub-systems; [4] *Exemplification: In order to achieve 4 marks a candidate should have described test procedures and obtained appropriate test results for 5 or more subsystems.*		
d	described and given the results of numerical (or other relevant) test procedures for the complete system; [2]		
e	performed relevant calculations; [2]		
f	evaluated the performance of sub-systems; [2]		

4. System construction:

The Candidate has:

		Mark	**See report page(s)**
a	worked safely, with an organised approach to system layout and planning. [3]		

5. Performance of the system:

The Candidate has:

a	produced a system whose sub-systems and the complete system worked well; [4] *Exemplification: In order to achieve 4 marks, a candidate should have produced a system which worked reliably. 2 marks may be obtained if 4 or more subsystems worked at some time.*		
b	produced a system whose initial specification and final performance agree well; [3] *Exemplification: In order to achieve 3 marks the initial specification and final performance should agree on 6 parameters or more.*		
c	evaluated the performance of the system against the initial specification and made relevant suggestions for further development. [4] *Exemplification: 2 marks may be obtained by making a full comparison of initial specification and final performance.*		

6. Initiative and creativity:

The Candidate has:

a	worked without support; [3]		
b	demonstrated organisation and diligence in the development of the project; [2]		
c	successfully attempted an enterprising project. [2]		

7. Communication:

The candidate has:

a	submitted a well-presented and structured account of the work done [3] *Exemplification: In order to achieve 3 marks a candidate should also have shown a high level of written communication with correct use of technical terms.*		

Total mark (Maximum 50)		

Guidance notes for Assessors:
The exemplification statements are intended to give an indication of the level of performance which will attract full marks. In most cases the exemplification covers a group of related but individual attributes. Intermediate performance can be credited for candidates who have fulfilled some of the requirements fully or partially met all/most of the requirements.