GCE EXAMINERS' REPORTS

ELECTRONICS
AS/Advanced

SUMMER 2014

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ELECTRONICS

General Certificate of Education

Summer 2014

Advanced Subsidiary/Advanced

ET1

Principal Examiner: Mr R A Blackmore

General comments:

The paper gave a very good coverage of the specification and was accessible to candidates of all abilities with a mark range of 0 to 60. There were very few omissions and all questions were answered correctly at some point. Following the recent trend, the sequential logic questions gained the lowest facility factor despite similar questions being asked previously. The exception was the down-counter question which was better understood than before.

Specific comments:

Q.1 A very straightforward introduction with most candidates gaining full credit. A few candidates mistakenly used $\overline{\mathrm{A.B}}$ in place of $\overline{\mathrm{A}}.\overline{\mathrm{B}}$ or gave the Boolean expression for an OR gate for $\mathrm{Q_3}$ even when they had the table correct.

Q.2 (a) Generally very well done although a few badly drawn diagrams made it difficult to distinguish between AND and OR gates. A few diodes in place of NOT gates were seen. In all there were about six possible circuits that could have gained this mark but those using NOR/NAND gates were not credited.

(b) Mostly good. Candidates who followed last year's advice to draw a faint circle around each replacement combination of NAND gates inevitably gained all 3 marks. Several candidates mixed up OR and NOR replacement circuits.

(c) Quite a number of mistakes were seen in the crossing out of redundancies, usually involving the AND gate pair.

Q.3 (a) As in the past, basic identities caused problems despite being listed in section 1.2.2 of the specification. In part (ii) one mark was awarded if candidates correctly expanded the bracket to produce 4 terms.

(b) Generally a good response. The most common mistake was to miss the $\mathrm{B}.\overline{\mathrm{C}}$ group that wraps around the table and identify two groups in its place. These candidates could gain ecf marks for the expression. As in previous years some obtained the correct solution from the Karnaugh map but then tried to simplify it further and incurred errors.

(c) Interestingly most candidates gained two marks for carrying out DeMorgan's theorem twice but then failed to simplify the resulting expression. A very common error was to incorrectly factorise the line $A+B+\overline{A}.B$ as $B(A+\overline{A})$, despite there being a standard simplification given on the data sheet on page 2. A few sensibly drew their own Karnaugh map to assist with the simplification.

Q.4 (a) The answers inverted were not enough to gain the mark. They had to make it clear that the circuit reset at logic 0 or else they used the words 'active low'. There were surprisingly few full mark answers. Many candidates chose A and C to reset the counter despite the fact 5 had to be displayed. The very rapid propagation of the signal through logic gates means that if the display is to have time to show 5 the counter needs to reset using B and C. Some candidates took the output from the driver rather than the counter.

(b) The question specifically asked about the display but many candidates answered in terms of the pulse producer or the counter. Where appropriate ecf was awarded in part (ii). Weak answers included: 'the display flashed' rather than scrolled through the numbers 0 to 5 very rapidly in (i) or 'nothing' instead of the display froze on a single number for part (ii).

(c) Few good answers seen. The answer to 'make it random' was not enough. Answers had to make it clear that the high frequency made the outcome (pseudo) random and therefore unpredictable. A significant number said this was slow enough to see the numbers.

Q.5 (a) The latching mark was only awarded if the setting/resetting was correct. This was to avoid random 1's and 0's gaining credit.

(b) There were rather more poor quality diagrams than one should expect at this level. These often had incorrect symbols for switches and resistors and/or wires connected to every point causing short circuits etc. Connections to $\overline{R}$ were ignored unless they prevented the setting of the circuit.

(c) The first mark was for the LED to be orientated so that it would function as an indicator of the output. The second mark was for $\overline{Q}$ sinking the current. A current limiting resistor is normally shown in this diagram but was not considered essential as the IC self-limits the current. Once again marks were lost for incorrect symbols such as diodes or photodiodes or diagrams with extra connections.

Q.6 (a) The $\overline{Q}$ to D connection ($\times 3$) had to be gained before the other marks were awarded. To gain the third mark the clock and output connections had to be compatible.

(b) Generally well answered with very few inversions.

Q.7 (a) Voltage gain should be dimensionless but very many candidates insisted on giving it a unit. This is normally treated benignly when marking but candidates should be very careful not to put in multipliers. The inverting amplifier value of 68 was commonly seen.

(b) Most candidates successfully extracted the correct value of pressure from the graph for part (i). For part (ii) many candidates simply gave the value for the input voltage, $V_{X,}$ instead of then multiplying this by the gain to get V_{OUT}. The 2 marks available should have been a clue that some processing of data was required.

(c) Very few correct answers were given here. Two frequent mistakes were to give the highest value from the pressure axis of the graph or to wrongly convert 8.0 V to 80 mV and read the answer as 120 kPa from the graph. A few mistook V_X for V_{OUT} and extrapolated the graph. For those candidates who did correctly calculate the maximum value for V_{IN} using the saturation voltage and gain the remaining marks were easily gained.

Q.8 (a) Few 3 mark answers were seen. A variable resistor had to be drawn in the feedback loop. Common mistakes were to show positive feedback or connections for a non-inverting amplifier.

(b) (i) The instructions made it clear that the value of feedback resistance had to be clearly identified **in the answer space**. Answers on the diagram were given credit this time but problems occur if the diagram itself is incorrect. Candidates must attempt to make their answers clear and unambiguous. Resistances should be 1 kΩ or greater but values of more than 10 MΩ should not gain credit.

(ii) Many scripts gave the value of input impedance for the op-amp from the table rather than using the value for R_{IN} they had chose in part (i).

(c) Both the correct value for the voltage gain and the minus sign were needed here.

(d) Most candidates got this frequently asked question correct. Once again careless use of units and/or multipliers cost a mark. Negative signs were ignored. A few candidates tried to multiply either the gain or the gain-bandwidth product by 0.7.

(e) The three marks were awarded independently and whilst there were relatively few text book answers many candidates were able to gain some credit.

ELECTRONICS

General Certificate of Education

Summer 2014

Advanced Subsidiary/Advanced

ET2

Principal Examiner: Mr D G Price

General comments:

The paper proved to be accessible for candidates of all abilities with an attempt rate per question ranging from 93.3 to 99.1%. Correct answers were obtained to all questions. The marks obtained ranged from zero to 100%.

Specific comments:

Q.1 This was the highest scoring question on the paper with a mean mark of 5 out of 6. It proved to be a nice gentle introduction which most candidates took full advantage of. A small minority of candidates struggled with part (e) and simply added the resistor values.

Q.2 In part (a) most candidates were able to calculate either V_{OC} or I_{SC} although R_O was often an ecf mark.

The equivalent circuit in (b) presented a problem for a significant number of candidates with a reluctance to show the load or to transfer values for V_{OC} and R_O to the diagram. Another common error was to use I_{SC} in both the diagram and the calculation. As long as the diagram was correct, part (b)(ii) was generally done well.

It was evident that a small number of centres had not covered Thevenin's theorem in any depth (if at all), as no attempt was made by virtually all candidates for those centres.

Q.3 (a) (i) Some candidates attempted to multiply or divide by $\sqrt{2}$, others subtracted a 1.4 V voltage drop.

(ii) The drawing of the half-wave rectified output was quite poorly done. A significant number of candidates drew full wave rectified outputs, and some drew smoothed outputs even though no smoothing capacitor was present.

(b) (i) The majority of candidates were able to correctly add the capacitor to the circuit diagram.

(ii) A significant number of candidates did not use the output they provided as an answer for part (a)(ii) as a basis for the smoothed output. A small number showed a very large voltage, ignoring the information given, that a small current was drawn from the system.

(c) Only a small number of candidates realised that the ripple voltage is double the mains frequency for full wave rectification.

Q.4 Parts (a) and (b) were quite well answered but a number of candidates used the charging rather than discharging formula and gained no marks.

In part (c) most candidates gained a mark for showing the bulb coming on after 20 seconds. Only the better candidates were able to relate the bulb going off with their answer to part (a).

Q.5 Part (a) was well answered.

In part (b) a significant number of candidates got the thresholds the wrong way round. Most candidates drew the correct graph. However common errors included: a non-inverted output, the incorrect amplitude and additional switching points.

Incorrect formula rearrangement resulted in quite a few candidates losing 2 marks in part (c).

Q.6. In part (a) most candidates gained 2 marks for the graph. A small number lost 1 mark by either failing to label the mark and space or reversing them.

Rearrangement of the formula was a problem for a number of candidates in parts (b) and (c).

Very few candidates realised that R_A was $2 \times R_B$ when the M-S ratio is 3:1.

Q.7 In part (a) most candidates scored at least 1 mark, but few scored all three. A combination of errors was evident: use of 12 V or 3 V instead of 9 V or 250 mA instead of 258 mA.

In part (b) although a large number of candidates gave 33 Ω [or an equivalent preferred value corresponding to the value calculated in part (a)] as the correct resistor, only the better candidates were able to explain that this was needed to ensure a minimum current of 8 mA through the zener diode to maintain the zener voltage.

Parts (c)(i) and (ii) were well answered .A common error in part (iii) was to use the original values of voltage and current to calculate the power rather than to substitute their answer to part (ii) into $P = \frac{V^2}{R}$.

Q.8 Most candidates had success in parts (a) and (b) although some misread the graph in part (b).

Part (c) was poorly answered but most candidates gained some ecf marks. Candidates tended not to subtract their answer to part (b)(ii) from 15 V to give the voltage across the 120 Ω resistor. Many candidates incorrectly used the formula $P = I^2R$ rather than $P = VI$ to calculate the power dissipated in the transistor.

Q.9 This was the lowest scoring question on the paper with a mean mark of 3 out of 7. Producing a circuit diagram to fully achieve a given specification proved to be too demanding for all but the best candidates.
The main issues were:

- the orientation of the light sensing unit;
- incorrect symbol for a LDR;
- incorrect symbol or placement of the variable resistor;
- a tendency to get the ratio of resistor values for the reference voltage sub-system reversed;
- resistor values less than 1 kΩ.

ELECTRONICS

General Certificate of Education

Summer 2014

Advanced Subsidiary/Advanced

ET3

Principal Moderator: Mr D G Price

General Comments

I would like to thank centres for their effort in presenting candidates' work for moderation, including the online recording of centre marks.

Several consortium based centres failed to include work from other centres within the consortium in their sample. The automatic sampling process should be overridden and work from all centres in the consortium included.

Consortium based centres should refer to the following sections of the Internal Assessment Manual:

- Section 2.12 Consortium arrangements;
- Section 4 Guidance for Consortium Arrangement.

It would be very helpful if centres did not place individual candidate's work in plastic envelopes. A more efficient approach would be to provide the Coursework Mark Booklet as an A3 booklet which could then double up as a wallet for holding the candidate's work securely.

In the vast majority of centres, candidates produced an excellent range of projects. Some of the work was outstanding.

A small number of centres seemed to have provided a very detailed framework for both the Ladder Logic and PIC projects resulting in all candidates within the centre producing very similar programs in both cases. Within the tight framework provided, the candidate's contribution was mainly limited to providing the data loaded into the registers. This approach must be avoided.

The assessment of the work was within tolerance in the majority of centres with only a small minority requiring adjustment to their marks. The main cause of adjustment was due to either a lack of understanding of some of the assessment criteria or centres tending to give candidates the benefit of the doubt on most borderline decisions.

Specific Comments:

The following points are made to highlight several of the more misunderstood criteria contained in the Coursework Mark Booklet:

Ladder Logic Programming

1b: A small number of centres awarded marks in this section despite no software switches being used.

1c3: This mark should only be given with supporting evidence. For example, if a specification states that an output is required to pulse at 2 Hz, then an appropriate mark-space ratio for the timer could be 0.3 : 0.2.

Micro-Controller Programming

1b1/2: This mark cannot be awarded for use of these commands in configuring the ports, as they are usually provided in the template.

2a3 To achieve this mark:

- the candidate should provide evidence to show how the final performance compared with the initial specification for the program. For example, timing a flashing LED with a stopwatch over several seconds to check for the correct frequency;
- the supervisor must acknowledge observing the testing stage to certify that the program is actually running as designed.

Some programs seen this year in the micro-controller section could not have run due to:

- calls to non-existent sub-routines;
- missing labels;
- misspelt commands etc.

These would have caused syntax errors at the compiling stage. Despite this, candidates (and sometimes the supervisor) claimed that the program worked to the specification.

ELECTRONICS

General Certificate of Education

Summer 2014

Advanced Subsidiary/Advanced

ET4

Principal Examiner: Mr A Beddoe

General comments:

The paper performed well with marks in the range 3 to 50 being obtained. A number of outstanding scripts that achieved full marks were observed. Overall I feel that the paper was similar in demand to previous papers, with scaffolding on some questions providing multiple entry points to the questions particularly for the less able candidates. There were a fewer number of tricky calculations that had follow through issues so there were fewer opportunities to be unable to answer questions because of a failure in the previous stages. I would therefore consider the paper to be slightly more accessible as proved by the fact that full marks were achieved by a number of candidates.

Specific comments:

Q.1 As has been traditional the first question is aimed at being a gentle introduction to the paper to warm up the candidates and settle them down. In this case the Schmitt trigger question caused many candidates some difficulty.

In (a)(i) a number of candidates incorrectly identified the Schmitt trigger as a non-inverting Schmitt, and lost a mark.

In (a)(ii) only a small minority of candidates were unable to identify the switching thresholds.

In (b) 1 mark was available for an output matching the type of Schmitt given in part (a)(i). Another mark was available for correct switching levels and another one for the saturation values. Most candidates were able to gain at least two marks out of the three available.

Q.2 This question was based on the simple radio receiver and superheterodyne receiver.

In (a) candidates were asked to draw the block diagram of a simple radio receiver. This was not as successful as one might expect since all functional blocks were provided, as a number of candidates were unable to sequence these correctly. The biggest issue was putting the RF Filter in the wrong place.

In (b)(i) candidates were asked to determine the new output frequencies present at the output of the superheterodyne mixer. Most candidates were able to give the sum and difference frequencies, but a number failed to give the correct units, or no units at all and as is normal when no unit is specified, base units are assumed, in this case Hertz.

In part (ii) candidates successful in determining the outputs of the mixer were generally successful at determining the intermediate frequency.

The completion of the block diagram was well done by most candidates. The most common error was to add an RF Filter or RF Amplifier at the output instead of the correct answer of AF Amplifier.

Q.3 This question based on the transmission of digital data, has been a high scoring question in previous examination papers.

In part (a) of this question the candidates had to correctly arrange the data and parity bit to gain access to the marks. A number of candidates lost marks because of inaccuracies in the data, and/or parity bit. There are also a large number of candidates that do not understand that the first action in the RS232 transfer is the start bit going from high to low, and that this is separate to the data. Labelling the appropriate part of the signal is impossible for candidates that do not understand this basic beginning process of the transmission.

In the second part of the question candidates were faced with a multiple parity bit system. Part (i) required candidates to determine the five parity bits needed for a data packet. In the main, most candidates apart from the weakest were able to complete this part successfully. A few correctly used the 'incorrect' parity and gained 1 ecf mark.

In part (ii) candidates needed to identify the location of an error in a different set of data and parity bits. A significant number of candidates were able to identify that P_2 was the failing bit, but then failed to change the logic state of P_2 in the corrected version for the last part of the question, choosing instead just to duplicate the incorrect data given in the question.

Q.4 This question revisited the concept of modulation index and bandwidth of FM radio signals.

In part (a) the modulation index was generally calculated correctly. Where mistakes were made it was to subtract the lower limit of the audio signal from the higher limit, giving a non-integer answer to the calculation.

In many cases this was repeated when calculating the bandwidth in (b). Where an incorrect answer for β was used in the formula $2(1+\beta)f_i$, then ecf marks were awarded. The main reason for candidates losing marks in the second part of this question was for not providing units for the answer in kHz.

Q.5 This proved to be a demanding question for many candidates as it has in previous papers. The Schmitt trigger has previously proved to be a question that has only been completed successfully by the more able candidates, and there was little evidence to disprove this observation. Candidates as a result tended to either score very well or very poorly on this question.

Despite providing further space for candidates to draw an equivalent potential divider circuit, there is still little evidence that candidates are using it, as when the candidates score poorly it is because the question has a single voltage written down with no evidence of any calculation, or circuit to show any working or understanding, or alternatively the question is omitted altogether.

In certain centres it is very apparent that the calculation of switching thresholds for Schmitt triggers is being very well taught and understood by candidates.

Q.6 This question provided a twist on the pulse modulation questions where candidates were asked to identify the modulation technique used and a possible input signal that could have produced the modulated output shown. Generally the candidates either did very well on this question or very poorly. It was evident that more candidates appeared to be able to attempt this question than in previous years as there were very few omits for this question.

The main reason candidates lost marks was in a lack of consistency in their possible input signal, often missing key transitions that were present in the modulated signal.

Q.7 This question centred on the performance of a PCM transmitter/receiver.

In part (a) candidates were asked to give the frequency of the PISO clock in a transmission unit. Given that sampling was at 8 kHz, and the ADC output was 10 bit, the minimum frequency for the PISO clock must be 80 kHz. Few candidates achieved this answer as many were incorrectly quoting the Nyquist Theorem and gave answers either half / double the sampling period for no marks. Marks for the explanation were only awarded if the PISO clock frequency was correct.

In part (b) candidates gained one mark for the correct use of 2^n, the second mark was for giving an answer of 5.86 mV. Main errors were showing no workings and rounding answers to just one / two significant figures leading to an imprecise answer for the resolution. Another common error was to neglect to put in the unit 'mV', leaving just a number which according to normal practice is interpreted as 'V' and hence was marked incorrect.

In part (c), only a few candidates were able to correctly construct the PCM receiver block diagram. Some candidates only scored 1 mark for linking the SIPO clock to the SIPO shift register. The weakest candidates were even unable to match these two units together.

Q.8 This question was designed to test the candidates understanding of filter circuits. This was a demanding question that had little success previously with many omissions of the question by candidates. The style of the question was modified this year to provide candidates with an approximate range of the answers required, and if they could not achieve this, an entry point for later parts of the question.

In (a)(i) the identification of the resonant frequency was accomplished by the majority of the candidates. In (a)(ii) the candidates needed to show on the graph how the bandwidth was calculated. There needed to be evidence of the candidates looking for $0.7 \times$ peak output voltage on the graph, with these points identified, the bandwidth would be 8 kHz. Some candidates used the answer to (b) to calculate the bandwidth for (a)(ii) this was 7.8 kHz and gained no marks.

Part (b) was meant to be quite straightforward, and candidates would have gained an ecf mark provided that they used the same numerical answers they gave in (a).

Part (c) proved to be difficult for a number of candidates as the formula needed rearranging to give the value of L, and this coupled with candidates being unsure how to deal with standard multipliers led many candidates astray. Candidates that did not use the given value of 60 for Q, gained no marks if their own answer in (b) was out of range.

Part (d) - those candidates that could handle the multipliers in part (c) were able to do part (d) quite comfortably, whilst the converse was also true, those that struggled with multipliers in the previous question also struggled here. With only one mark available for the question no ecf could be applied.

In part (e) there were a number of candidates that were able to do part (i) since all the values needed were provided in different parts of the question. When it came to part (ii) a significant majority of candidates had no idea what to do, and there were a significant number of omits on this part of the question.

ELECTRONICS

General Certificate of Education

Summer 2014

Advanced Subsidiary/Advanced

ET5

Principal Examiner: Mr J Verrill

General comments:

The performance of candidates in the top half of the mark range showed a significant improvement over previous years. As ever, many marks were lost because candidates failed to read the question or interpret correctly the information in it. A typical example of this is Q3(b)(i) where the name of the Interrupt Service Routine was given earlier in the stem of the question, but was missed by many.

As mentioned in previous reports, many marks were lost as a result of illegible handwriting, misuse of circuit symbols, missing or incorrect units and badly drawn graphs and diagrams (without the use of a pencil and ruler, for example). Inability to write cogent and concise explanations led to low marks in questions 3 and 5, for example.

As before shading portions of graphs risks hiding features which would otherwise gain marks. When drawing signals on graphs, it is best to label significant values and synchronise related graphs using vertical lines (in Q7(c) for example,) to ensure that marks are awarded. As before, it is sad to see that many candidates are seemingly happy to quote, without qualification, output voltages well in excess of power supply values, e.g. "146.75 V", "-139.63 V" etc.

Q.1 A minority drew only the main sequence in answering part (a). Others included the unused states but did not show how they were connected to the main sequence, a requirement implicit in the instruction "Complete the state diagram..." Another common mistake was to omit '000' from the unused states.
In part (b), a very common mistake was the expression:

$$D_A = \overline{\overline{A} \,.\, C}$$

missing the addition of 'B' to the expression. Many scored full marks, and most over half marks on this question.

Q.2 Equally accessible, most candidates scored highly on this question.

In part (a), a common mistake was to list the main sequence (in states 0 to 4,) and then repeat the first part of it in states 5 to 7. The instruction said "Complete the table for **all eight** possible output combinations..."

'Error-carried-forward' (ecf) in parts (b) and (c) meant that mistakes in part (a) did not necessarily lose marks throughout the question.

In part (c), there was a suspicion that some candidates are confusing the terms 'unused' and 'stuck' states.

Q.3 As in previous years, performance on microcontrollers seems to depend on the centre more than on the individual candidate.

In part (a), there were problems once more with the code needed to configure ports, even though this was a necessary part of the coursework in module ET3. The use of blank spaces, or 'x' was penalised, unless defined by the candidate, as 'don't care' values, as the question required the actual code that would be used.

In part (b), many lost the mark in (ii) through having a permanent connection from pin RB0/INT to 0 V. Some 'littered' the diagram with unwanted connections, which were ignored in marking unless they prevented initiation of the interrupt.

In (iii) a poor standard of explanation hampered many. The role of 'INTCON,1' is to show which type of interrupt took place - an external interrupt on RB0/INT in this case. It must be cleared within the Interrupt Service Routine (ISR) to avoid constant repetition of the ISR.

Part (iv) required three elements in the answer - what happened to the buzzer during the ISR, what happened to the LED during the ISR, and the role of the switch attached to Port A, bit 0. Many answers missed out, or misunderstood what took place with these.

Q.4 Performance on this question was mixed.

In part (a), there were many correct answers, but some had them in the wrong order, i.e. (i) had the answer for (ii) and vice-versa. Some answers were too vague, talking about 'output' and 'input' without specifying current or voltage.

It is sad to report that many did not know the correct symbol for a transistor, needed in part (b). Often, the arrow identifying the emitter was missing. Part (i) needed the candidate to recognise that the voltage at the non-inverting input was simply the zener voltage - no calculation needed. The Information Sheet contained the formula needed for part (iii). Some knew little about voltage regulation, and produced incorrect or meaningless answers to part (iv). Correct answers were expected to contain a reference to the voltage across the 180 Ω resistor. Some talked vaguely about "...the resistor(s)..."

Q.5 Part (a) revealed surprising weaknesses in understanding, and powers of explanation.

In (i), some focussed on the word 'Gray', mistaking it for the colour 'grey' and made statements about detecting colours or patterns. Others believed that Gray code was analogue, while binary code was digital!

Answers to (ii) were expected to concentrate on the pendulum moving from one segment to an adjacent one, with the potential for errors in the binary code resulting from misalignment of optoswitches or segment boundaries.

Part (b) was generally very well answered.

Q.6 For many, parts (a) and (b) seemed to be a lucky dip, choosing between answers of 'increase', 'decrease' or 'stay the same'. Better answers showed evidence of some calculation or reasoning.

Part (c) produced the weakest performance of any question on the paper. Too many answers focussed on the meaning of CMRR, without applying it to this particular application, as the question required. Implicit in many answers was a confusion between the role of the op-amp and that of the dummy strain gauge, which complement each other in reducing effects like temperature change. The signal from the bridge circuit can be thought of as containing two elements - the strain information, (a very small voltage signal) and a much larger DC excitation voltage. The latter is common to both legs of the bridge, and should be cancelled out in the amplifier. For this to happen, the amplifier needs a high CMRR. Some of the better answers talked about eliminating noise, picked up by the wires connecting the bridge to the amplifier.

Part (d) relied on the difference amplifier formula, given in the Information Sheet. Some quoted only the difference in the voltages at X and Y, while others subtracted these in the wrong order, and gave a negative answer.

Q.7 Thyristor control continues to cause problems!

Part (a) should have been a straightforward introduction. However, too many confused the circuits for AC phase control with DC control; many could not draw the correct circuit symbol for a diac; many overlooked the requirement that the brightness of the lamp should be variable.

In part (b)(i), it appeared that some have never had to carry out this kind of calculation before. A surprising number used the value of the capacitance directly, instead of the capacitive reactance, in the phase angle formula. Some seemed unable to use a calculator (or did not have one) to generate the answer.

Most answers to part (c) showed elements of being correct, but had errors such as the value of the firing voltage. Better candidates labelled this as 25 V, or had a dotted line linking it with the upper graph.

Q.8 Part (a)(i) required that the product of the gains of P and Q equalled 100. However, many used the sum of the gains. To maximise bandwidth, the gains should be equal (and so equal 10).

In (ii), the gain used should have been the higher of the P and Q gains (and so equal to 10.) However, the majority of candidates used the overall voltage gain of the system (equals 100). Many recognised the function of the capacitors in part (iii).

In part (b)(i), two wrong answers indicated particularly worrying aspects of the understanding of amplifiers. The first was the answer of infinite gain, the second of zero gain! Probably around half of the candidates correctly recognised the gain to be unity.

In (ii), most answers were incorrect, suggesting inversion of the signal, or some need to further amplify it. Impedance matching was mentioned by a small minority, with even fewer focussing on the reduction in output impedance.

Q.9 This resulted in high scores for most candidates.

Most produced correct sketches of the filter characteristics, in part (a), and the corresponding circuit diagram in (b)(i). There were variations, particularly in the placing of the capacitor, but allowing ecf in part (b)(ii) reduced the impact of these mistakes. The answers to (ii) were often muddled, hiding the chosen value of capacitance. The following was a common mistake:

$$1 \times 10^{-10}\text{F} = 10\,\text{nF}$$

The most common answer to (c)(i) was 1.9 V (either '+' or '-'), meaning that the candidate had ignored the 0.7 V drop across the emitter follower. The sketches offered for part (ii) were often too inaccurate to gain full credit, even though elements of correct reasoning could be seen. This is a case where voltage labels would have helped greatly in clarifying what the candidate intended.

Q.10 Many used the formula given in the Information Sheet correctly, though some ignored the '-' sign.
Only a minority scored full marks in (b)(i). The common mistake was to halve, not double, resistor values for R_A and R_B. Even fewer calculated the value of R_F correctly.
The two requirements for a correct answer to (ii) were an inverting voltage amplifier circuit, and unity voltage gain (meaning equal values for R_F and R_{IN}.) The performance was disappointing, with only a minority scoring both marks.

ELECTRONICS

General Certificate of Education

Summer 2014

Advanced Subsidiary/Advanced

ET6

Principal Moderator: Mr D G Price

General comments:

I would like to thank centres for their effort in presenting candidates' work for moderation, including the online recording of centre marks.

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It would be very helpful if centres did not place individual candidate's work in plastic envelopes. A more efficient approach would be to provide the Coursework Mark Booklet as an A3 booklet which could then double up as a wallet for holding the candidates' work securely.

Candidates produced an excellent range of projects and some of the work seen was outstanding.

The majority of centres provided both excellent annotation and excellent photographic evidence, which aided the moderation process.

The assessment of the work was within tolerance in the majority of centres with only a small minority requiring adjustment to the marks.

Specific comments:

The following points are made to highlight several of the more misunderstood criteria contained in the Coursework Mark Booklet:

1. Initial specification
   Some specifications tended to be more a list of sub-systems required rather than an actual specification of a system. Several centres gave credit for power supply voltage / current requirements even when there was no justification provided for the values chosen. A full specification should include measurable parameters.

2. Project planning and research
As reported in previous years, centres tended to be generous in awarding these marks. It is expected that candidates will make use of their theory notes and information provided in the WJEC notes as a matter of course. Searching the internet / text books for the circuit diagram and frequency formula of a 555 astable / monostable as well as readily available datasheets is not relevant research. Several centres are accepting references to the course notes provided by the WJEC as relevant research.

3. Project development
Candidates from a small number of centres were given credit for single logic gate sub-systems, possibly in an attempt to access the marks available for "5 or more sub-systems". At this level a logic gate would normally form part of a larger sub-system. For example, a NOT gate used to invert the output of a monostable should not be considered as a sub-system. It should form part of the monostable sub-system. Alternative sub-systems must be viable / practical for the chosen application.

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