GCSE Examiners' Report

Subject: Electronics

Level: GCSE

Summer 2024

Introduction

Our Principal examiners' report provides valuable feedback on the recent assessment series. It has been written by our Principal Examiners and Principal Moderators after the completion of marking and moderation, and details how candidates have performed in each component.

This report opens with a summary of candidates' performance, including the assessment objectives/skills/topics/themes being tested, and highlights the characteristics of successful performance and where performance could be improved. It then looks in detail at each unit, pinpointing aspects that proved challenging to some candidates and suggesting some reasons as to why that might be.[1]

The information found in this report provides valuable insight for practitioners to support their teaching and learning activity. We would also encourage practitioners to share this document – in its entirety or in part – with their learners to help with exam preparation, to understand how to avoid pitfalls and to add to their revision toolbox.

Further support

Document	Description	Link
Professional Learning / CPD	Eduqas offers an extensive programme of online and face-to-face Professional Learning events. Access interactive feedback, review example candidate responses, gain practical ideas for the classroom and put questions to our dedicated team by registering for one of our events here.	https://www.eduqas.co.uk/home/professional-learning/
Past papers	Access the bank of past papers for this qualification, including the most recent assessments. Please note that we do not make past papers available on the public website until 12 months after the examination.	Portal by WJEC or on the Eduqas subject page
Grade boundary information	Grade boundaries are the minimum number of marks needed to achieve each grade. For unitised specifications grade boundaries are expressed on a Uniform Mark Scale (UMS). UMS grade boundaries remain the same every year as the range of UMS mark percentages allocated to a particular grade does not change. UMS grade boundaries are published at overall subject and component level. For linear specifications, a single grade is awarded for the subject, rather than for each component that contributes towards the overall grade. Grade boundaries are published on results day.	For unitised specifications click here: Results and Grade Boundaries and PRS (eduqas.co.uk)

[1] ***Please note that where overall performance on a question/question part was considered good, with no particular areas to highlight, these questions have not been included in the report.***

Exam Results Analysis	Eduqas provides information to examination centres via the WJEC Portal. This is restricted to centre staff only. Access is granted to centre staff by the Examinations Officer at the centre.	Portal by WJEC
Classroom Resources	Access our extensive range of FREE classroom resources, including blended learning materials, exam walk-throughs and knowledge organisers to support teaching and learning.	https://resources.eduqas.co.uk/
Bank of Professional Learning materials	Access our bank of Professional Learning materials from previous events from our secure website and additional pre-recorded materials available in the public domain.	Portal by WJEC or on the Eduqas subject page.
Become an examiner with WJEC.	We are always looking to recruit new examiners or moderators. These opportunities can provide you with valuable insight into the assessment process, enhance your skill set, increase your understanding of your subject and inform your teaching.	Become an Examiner | Eduqas

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Executive Summary

Candidates' performance in GCSE Electronics this year, was broadly in line with previous years. The mean mark for Component 1 (exam) was slightly lower than 2023; the mean mark for Component 2 (exam) was slightly higher. The mean mark for Component 3 (NEA) was slightly lower than 2023. The standard deviation of marks for all three components was very similar to previous years.

Analysis of responses to questions showed the level of difficulty of the Component 1 and 2 exams to be similar to 2023.

Component 1: Discovering of Electronics (exam)

Candidate performance was good overall, with some excellent answers to questions. Candidates attempted the majority of questions. The QER question was most often omitted and candidates scored fewest marks on this question. Quality of presentation by some candidates was poorer than previous years.

Component 2: Application of Electronics (exam)

The mean mark in this component was less than that of Component 1. This is usually the case, reflecting the more applied nature of questions in this paper. However there were also some excellent answers to questions in this exam.

Component 3: System Design and Realisation Task (NEA)

As in previous years, work presented for moderation was well organised. Examples were seen of well-planned and developed circuits. Many physical circuits were well laid out and thoroughly tested, with good photographic evidence provided.

Work was accurately marked by most centres, with only a small number of centres' marks requiring adjustment. NEA requirements are generally well understood however centres should note that candidates' work must be based on an individually identified problem. Clear annotation of candidates' work, indicating which marking criteria have been achieved, is helpful in justifying marks awarded.

Areas for improvement	Classroom resources	Brief description of resource
Quality of response (QER) questions.	GCSE Electronics eBook	Chapters cover the full content of the specification with worked examples, exercises and practical investigations for each topic.
	Knowledge organisers	Concise summary of each topic, to assist with planning answers to QER questions.
	Past papers and mark schemes	Past papers and mark schemes (available on Portal) contain examples of QER questions and answers.
	CPD material	CPD material on Portal contains commentary from previous series and examples of answers.
NEA – The specification should give details of an individually chosen problem.	GCSE Electronics specification	Description of the NEA requirements and marking criteria.
	Guidance for Teaching	Further guidance on the NEA with an exemplar project, marked and annotated.
	CPD material	CPD material on Portal contains commentary from previous series and examples of work.

ELECTRONICS

GCSE

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Component 1 – Discovering Electronics

Overview of the Component

This component is aimed at testing the fundamental concepts of Electronics. The exam is broken down into small parts to test multiple factors of candidates' knowledge of the essential topics needed to progress in the subject. Candidate performance in this component was good overall, with some excellent answers observed across the whole range of questions. A small minority of candidates achieved very few marks as much of their scripts were left blank. In contrast a small number achieved near full marks.

The question paper was broken down into 44% (AO1), 44% (AO2) and 12% (AO3).

The topics tested were

1. Basic Logic Gates / Truth Tables.
2. System design using a functional block approach.
3. Use of Ohm's Law and Resistor Colour Code / Circuit Voltage / Current rules.
4. Completion of Truth Tables / Conversion of a logic circuit to NAND gates.
5. Sensing Circuits using Operational Amplifier
6. Applications of D-Type flip-flops
7. Transistor Switching Circuits
8. Regulated Power Supplies

The overall performance on the paper was good with an overall mean mark of 47.7 for matched candidates (similar to the pre-pandemic 2019 performance) and 48.7 for all candidates (lower than the similar performance in 2019).

In comparison to 2023, there was a fall in the mean of 1.3 marks for matched candidates and 3.3 for all candidates. Across all candidates, marks ranged from 1 to 80.

In general candidates attempted the majority of questions. The largest omission was the QER question, which tested the ability of candidates to analyse and evaluate a circuit design and communicate their understanding in extended prose.

The quality of presentation in some candidates' answers was quite poor compared to previous years. For example diagrams drawn in ink instead of pencil, multiple crossing out and no attempt to redraw a messy diagram on the spare pages. The use of a ruler was sparse and when it was used, some candidates were unable to follow graph paper grids accurately.

Comments on individual questions/sections

Q.1 A successful question for the majority of candidates. A few lost marks in part (b) for naming the gate corresponding to the truth table instead of which IC package contained that specific gate.

Q.2 A number of candidates seemed to be unaware of the function of the given functional blocks. Sorting these into input / processing / output blocks was poor, leading to difficulties in constructing a working block diagram to meet the specification.

Q.3 The Resistor Colour Code was well understood. Circuit rules for voltage and current are not well understood by a large number of candidates. Many candidates mixed up the relevant units (Volts, Amps and Ohms) for basic circuit parameters.

Q.4 A number of candidates struggled with the completion of the Truth Table Conversion. Several candidates do not know the NAND equivalent circuits for standard Logic gates making identification of double inversions impossible.

Q.5 Some candidates found it hard to complete the comparator design correctly and even when given specific conditions for the comparator inputs, could not determine the output.

Q.6 The applications of D-Type flip-flops formed the synoptic part of this paper and had a mixed response from candidates.

Q.7 The transistor switch is not well understood by a large number of candidates. Many were unable to perform the appropriate calculations related to the design, to verify its functionality.

Q.8 The basic operation of the Zener diode to produce a regulated voltage was not well understood by a number of candidates. In this QER question, many candidates did not know how to analyse the circuit. Far too many candidates tried to use the Power of the Zener and Resistor to determine current flow, showing misunderstanding of this particular circuit.

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Component 2 – Application of Electronics

Overview of the Component

This component is aimed at testing the application of electronics in larger systems. It requires candidates to apply knowledge of basic building blocks to their function in a larger systems.

Candidate performance in this component was poorer than that in Component 1, reflecting the fact that this paper is based more on application of knowledge to whole systems rather than recall questions. A number of low marks were observed, however there were also a number of excellent answers across the whole range of questions.

The question paper was broken down into 44% (AO1), 44% (AO2) and 12% (AO3).

The topics tested were

1. Flowcharts as part of a larger control system.
2. 555 Monostable circuits
3. Binary Counters / 7 segment displays
4. Inverting amplifiers.
5. Schmitt Inverter.
6. Divide by 2 counter.
7. Use of an oscilloscope to determine amplitude, period and frequency of an astable circuit. Analysis of 555 Astable circuit and corresponding output graphs.
8. Non-inverting Amplifier
9. MOSFET driver circuit
10. Operation of a Decade Counter

The overall performance of the paper was in line with previous performance of candidates. The overall mean mark was 43.0 for matched candidates and 45.1 for all candidates. Both are higher than the mean achieved in 2019 pre-pandemic.

In comparison to 2023, there was an increase in the mean of 4.7 marks for matched candidates and 3.3 for all candidates.

These mean scores are however lower than the comparative means for Component 1, reflecting the much higher demand of dealing with large systems, requiring application of understanding rather than straight recall. Despite this, across all candidates, marks ranged from 0 to 80.

The quality of presentation by some candidates was also poor compared to previous years, as in Component 1.

Comments on individual questions/sections

Q.1 No specific areas to highlight.

Q.2 Most candidates were able to select the appropriate formula for a 555 monostable and determine the minimum time delay. In attempt to determine the setting of the variable resistor, a number of candidates neglected to subtract the value of the fixed resistor to complete the calculation. The description of what happens at the output when the switch was pressed was poor, with many candidates not referring to the output at all.

Q.3 No specific areas to highlight.

Q.4 When attempted, this question was answered well and the candidates showed a good understanding of the inverting amplifier.

Q.5 The most significant errors in this question were caused by the lack of a ruler and / or inability to follow the graph paper grid lines accurately, resulting in the incorrect threshold switching points being identified.

Q.6 In many cases, candidates did not recognise that the divide by 2 counter was needed to ensure that the correct number of laps was counted i.e. the two pulses from front and back wheels had to be counted as one. Again a lack of care in using the grid lines to draw the output graphs resulted in marks being lost by candidates.

Q.7 Some candidates were unable to interpret the oscilloscope trace correctly. There was some confusion over the amplitude measurement even though this has been clarified many times. Candidates also showed confusion about what units to give with their answers for amplitude (V) and period (ms). Some candidates struggled to obtain the correct ‘mark’ & ‘space’ times using the formulae for a 555 Astable as they couldn’t apply the multipliers ‘k’ and ‘µ’ correctly.

Q.8 No specific areas to highlight.

Q.9 Candidates who understood the application of the MOSFET scored well but there were a lot of omissions and zero marks on this question.

Q.10 Most candidates were able to give the Boolean expression for the yellow and orange outputs. There was less success with completing the truth table, with candidates failing to spot that Q5 resets the decade counter.

Component 3: Extended system design and realisation task (NEA)

Overview of the Component

The NEA is an integral part of the WJEC Eduqas GCSE in Electronics. This component requires each candidate to produce a single extended system design and realisation task independently. This builds on the systems developed throughout the specification and the requirement to relate practical circuit design and construction to knowledge and understanding from Components 1 and 2.

Centres must be thanked for their effort in presenting candidates' work for moderation, and for recording the marks online.

The assessment of the work was within tolerance for most centres this year but for some centres, adjustments to marks were required.

Comments on tasks/questions relating to candidate performance/meeting assessment criteria

System Planning

Design specifications should contain a range of both qualitative and quantitative terms based on the candidate's analysis of the problem. To access the higher mark band, the specification should contain detailed, measurable electronic parameters.

Unless very good reasons are provided as justification, neither the battery supply voltage nor the number of components should be considered as quantitative specifications.

In some centres candidates included research into components which are included in the WJEC specification for components 1 and 2. This research should not be credited as relevant research. Examples of research that was relevant to the specification concentrated on quantitative specifications – such as finding the optimum temperature for an egg incubator or finding the legal limits for a car alarm sounding duration.

System Development

Many candidates carried out a high standard of rigorous sub-system testing. These candidates set up their sub-systems on breadboard and showed excellent photographic evidence of the test instruments used. The results were then analysed logically.

Some accounts however tended to be observational, with limited records of the testing that took place. For each sub-system a test reading should be provided with the output activated and non-activated.

Centres that choose to carry out tests on circuit simulations should note that results are only valid if the actual components used in the real circuit are tested. This means that test results obtained using generic components such as IC1 and Q1 should not be credited as valid tests. When using a flowchart program, simulation tests should be carried out for the program and include screenshots of the results.

System Realisation

Candidates generally either produced their circuits on PCB or on breadboard. If candidates produce the final circuit on PCB, then layout diagrams showing their modifications to the software generated layouts must be included. Similarly, either a clear photo, or a diagram of the plan layout should be included for a breadboard.

To gain the full range of marks for system realisation, candidates must have a very well organised physical circuit layout (rather than a circuit diagram), with wires and components arranged vertically/horizontally to a high standard.

As was the case with sub-system testing, many candidates this year conducted a high standard of final circuit testing, using appropriate test equipment and included clear photographic evidence of the actual testing taking place. They gave in depth analysis and comparison of their numerical results with their quantitative specifications.

The majority of candidates provided excellent photographic evidence showing their final circuits in operation. This was an effective way of demonstrating their circuits working reliably.

Some of the testing however, tended to be observational with limited use of test equipment. The recording of test results tended to lack detail and the analysis of the results was superficial. Marks were sometimes awarded for reliable operation of 3 sub-systems when glaring errors could be seen in the circuits.

Most centres provided excellent photographic evidence of the candidates' finished circuits. In a minority of reports, photographs were too small for details to be legible.

Evaluation

Good practice evaluations made valid, critical and objective assessments of performance, compared with numerical design specifications.

Some centres over awarded marks in this category because the original specification did not have realistic measurable parameters. This resulted in simplistic evaluations.

Many candidates made sensible, realistic suggestions for improvements, with explanations. To access the higher band, candidates must explain how their suggestions would lead to improvements.

Task marking
Comments on approaches to internal marking

Some centres provided candidates with a prescriptive template. This should be avoided as this guidance can limit the mark awarded to candidates.

Most centres provided annotation of candidates work. Centres that did not provide annotation this year should consider providing an indication on the mark scheme of which level descriptors were achieved. This would be very helpful in justifying marks awarded by the centre during the moderation process.

The candidates of most centres produced a very good range of projects. However, in some centres all candidates' work seemed to have focused on a common theme. Candidates should focus on their individually identified problem to enable them to write a design specification.

Awarding accurate marks is critical to ensure that candidates receive fair and consistent reward for the work produced. Banded mark descriptors help to determine the correct band where a candidate's work fits. Some centres awarded top band marks for System Development when there were less than five different sub-systems developed. Testing two very similar sub-systems such a red LED and a green LED as outputs should not be credited as two separate tests.

Supporting you

Useful contacts and links

Our friendly subject team is on hand to support you between 8.30am and 5.00pm, Monday to Friday.
Tel: 029 2240 4254
Email: electronics@eduqas.co.uk
Qualification webpage: Eduqas GCSE Electronics

See other useful contacts here: Useful Contacts | Eduqas

CPD Training / Professional Learning

Access our popular, free online CPD/PL courses to receive exam feedback and put questions to our subject team, and attend one of our face-to-face events, focused on enhancing teaching and learning, providing practical classroom ideas and developing understanding of marking and assessment.

Please find details for all our courses here: https://www.eduqas.co.uk/home/professional-learning/

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