GCE A LEVEL

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WJEC Eduqas GCE A LEVEL in

ELECTRONICS

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DESIGNATED BY QUALIFICATIONS WALES

SAMPLE ASSESSMENT MATERIALS

Teaching from 2017
For award from 2019

Version 2

wjec
cbac

SUMMARY OF AMENDMENTS

Version	Description	Page number
2	Amendments to PIC information, command and number system notation.	8

For teaching from 2017
For award from 2019

GCE A LEVEL ELECTRONICS

SAMPLE ASSESSMENT MATERIALS

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Contents

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WJEC Eduqas A level in Electronics

Data booklet

A clean copy of this booklet should be issued to candidates for their use during each A Level Electronics examination.

Centres are asked to issue this booklet to candidates at the start of the A Level Electronics course to enable them to become familiar with its contents and layout.

Preferred values for resistors

The figures shown below and their decade multiples and sub-multiples are the E24 series of preferred values.

10, 11, 12, 13, 15, 16, 18, 20, 22, 24, 27, 30, 33, 36, 39, 43, 47, 51, 56, 62, 68, 75, 82, 91.

Standard multipliers

Prefix	Multiplier
T	$\times 10^{12}$
G	$\times 10^{9}$
M	$\times 10^{6}$
k	$\times 10^{3}$

Prefix	Multiplier
m	$\times 10^{-3}$
μ	$\times 10^{-6}$
n	$\times 10^{-9}$
p	$\times 10^{-12}$

Useful equations

$$C = \frac{Q}{V}$$

$$I_C = h_{FE} I_B$$

$$\frac{1}{C} = \frac{1}{C_1} + \frac{1}{C_2}$$

$$I_D = g_M (V_{GS} - 3)$$

$$C = \frac{C_1 C_2}{C_1 + C_2}$$

$$P = I_D^2 r_{DSon}$$

$$C = C_1 + C_2$$

$$A + \overline{A} . B = A + B$$

$$V_{rms} = \frac{V_0}{\sqrt{2}}$$

$$A . B + A = A . (B + 1) = A$$

$$I_{rms} = \frac{I_0}{\sqrt{2}}$$

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$$G = \frac{V_{OUT}}{V_{IN}}$$

$$G = 1 + \frac{R_F}{R_1}$$

$$G = -\frac{R_F}{R_{IN}}$$

$$V_{OUT} = -R_F\left(\frac{V_1}{R_1} + \frac{V_2}{R_2} + ...\right)$$

$V_{OUT} = V_S$ for $V_+ > V_-$

$V_{OUT} = -V_S$ for $V_+ < V_-$

$V_{OUT} = V_{IN}$

$$\text{slew rate} = \frac{\Delta V_{OUT}}{\Delta t}$$

$$\text{slew rate} = 2\pi f V_P$$

$$\text{resolution} = \frac{\text{i/p voltage range}}{2^n}$$

$$X_C = \frac{1}{2\pi f C}$$

$$X_L = 2\pi f L$$

$$Z = \sqrt{R^2 + X^2}$$

$$f_0 = \frac{1}{2\pi\sqrt{L\,C}}$$

$$R_D = \frac{L}{r_L C}$$

$$Q = \frac{f_0}{\text{bandwidth}} = \frac{2\pi f_0 L}{r_L}$$

$$N_{CH} = \frac{\text{available bandwidth}}{\text{channel bandwidth}}$$

$$\text{maximum data rate} = 2 \times \text{available bandwidth}$$

$$G_{dB} = 10\log_{10}\frac{P_{OUT}}{P_{IN}}$$

$$SNR_{dB} = 10\log_{10}\frac{P_S}{P_N} = 20\log_{10}\frac{V_S}{V_N}$$

$$m = \frac{(V_{max} - V_{min})}{(V_{max} + V_{min})} \times 100\%$$

$$\beta = \frac{\Delta f_c}{f_i}$$

$$\text{Bandwidth} = 2(\Delta f_0 + f_i) = 2(1+\beta) f_i$$

$$c = f\lambda$$

$$V_{OUT} = V_{DIFF}\left(\frac{R_F}{R_1}\right)$$

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$$T = RC$$

$$V_C = V_0\left(1 - e^{-\frac{t}{RC}}\right)$$

$$V_C = V_0 e^{-\frac{t}{RC}}$$

$$t = -RC\ln\left(1 - \frac{V_C}{V_0}\right)$$

$$t = -RC\ln\left(\frac{V_C}{V_0}\right)$$

$$f \approx \frac{1}{RC}$$

$$f = \frac{1}{T}$$

$$T = 1.1RC$$

$$t_H = 0.7(R_1 + R_2)C$$

$$t_L = 0.7R_2C$$

$$f = \frac{1.44}{(R_1 + 2R_2)C}$$

$$\frac{T_{ON}}{T_{OFF}} = \frac{R_1 + R_2}{R_2}$$

$$V_r = \frac{I}{f_r C}$$

$$V_L \approx V_Z\left(1 + \frac{R_F}{R_1}\right)$$

$$\phi = \tan^{-1}\left(\frac{R}{X_C}\right)$$

$$f_b = \frac{1}{2\pi R C}$$

$$V_{OUT} \approx V_{IN} - 0.7$$

$$V_{OUT} \approx V_{IN} - 3$$

$$P_{MAX} = \frac{V_S^{\,2}}{8R_L}$$

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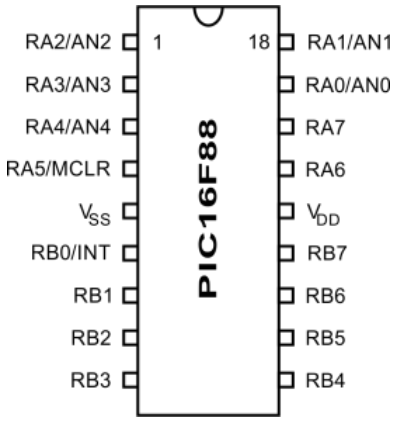
PIC Information

The PIC programs include 'equate' statements that define the following labels:

Label	Description
PORTA	input / output port A
PORTB	input / output port B
TRISA	the control register for port A
TRISB	the control register for port B
STATUS	the status register
INTCON	the interrupt control register
W	Destination d = W, result stored in working register
F	Destination d = F, result stored in specified file register
RP0	the register page selection bit 0
Z	the zero flag status bit
GIE	the global interrupt controller bit
INT0IF	the external interrupt enable bit

Pinout for 16F88 PIC IC:



List of commands:

Mnemonic	Operands	Description
addlw	k	Add working register to literal k
andlw	k	AND working register with literal k
bcf	f, b	Clear bit b of file register f
bsf	f, b	Set bit b of file register f
btfsc	f, b	Bit test bit b of file register f, skip if clear
btfss	f, b	Bit test bit b of file register f, skip if set
call	label	Call subroutine at label
clrf	f	Clear file register f
comf	f, d	Complement file register f
decfsz	f, d	Decrement file register f, skip if zero
goto	label	Unconditional Branch to label
incf	f, d	Increment file register f
iorlw	k	Inclusive OR working register with literal
movf	f, d	Move file register f
movlw	k	Move literal to working register
movwf	f	Move working register to file register f
nop	-	No Operation
retfie	-	Return from interrupt service routine and set global interrupt enable bit GIE
return	-	Return from Subroutine
sublw	k	Subtract W from literal

Number system notation

Decimal	d'153'
Hex	h'99''
Binary	b'10011001'

Structure of the INTCON register

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
GIE	PEIE	TMR0IE	INT0IE	RBIE	TMR0IF	INT0IF	RBIF

Structure of the STATUS register

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
IRP	RP1	RP0	$\overline{TO}$	$\overline{PD}$	Z	DC	C

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Candidate Name	Centre Number					Candidate Number				

A LEVEL ELECTRONICS

COMPONENT 1

Principles of Electronics

SAMPLE ASSESSMENT MATERIAL

2 hours 45 minutes

For Examiner's use only		
Question	**Maximum Mark**	**Mark Awarded**
1.	9	
2.	14	
3.	17	
4.	6	
5.	18	
6.	22	
7.	12	
8.	13	
9.	11	
10.	8	
11.	10	
Total	140	

ADDITIONAL MATERIALS

In addition to this examination paper,
you will require a calculator and a **Data Booklet**.

INSTRUCTIONS TO CANDIDATES

Use black ink or black ball-point pen.
Answer **all** questions.
Write your name, centre number and candidate number in the spaces at the top of this page.
Write your answers in the spaces provided in this booklet.

INFORMATION FOR CANDIDATES

The number of marks is given in brackets at the end of each question or part-question.
The assessment of the quality of extended response (QER) will take place in question **11(a)**.

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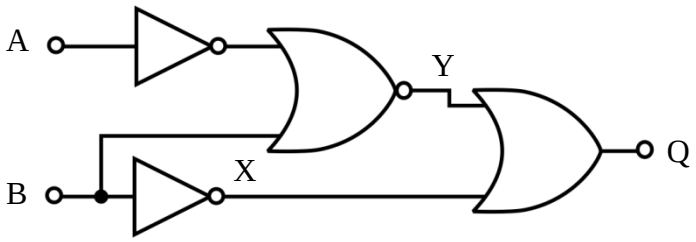
Answer **all** *questions.*

1. *(a)* Write down Boolean expressions for outputs X, Y and Q **in terms of the inputs A and B** for the following logic system. [3]



X = ...

Y = ...

Q = ...

(b) In the space below, redraw and simplify the logic system, using NAND gate equivalents. [6]

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2. *(a)* A student is asked to draw the truth table for the equation:

$$Q = \overline{\overline{(A+B)}+C}$$

Show how De Morgan's theorem can be used to simplify the task and draw the resulting truth table for the equation. [5]

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(b) In designing a logic system, a student has produced the Karnaugh map shown below.

DC \ BA	00	01	11	10
00	0	0	1	1
01	1	1	0	0
11	1	1	0	1
10	0	0	1	1

Give the simplest Boolean expression for the output Q of this logic system. On the Karnaugh map, **show** and **identify** the groups that you create. [4]

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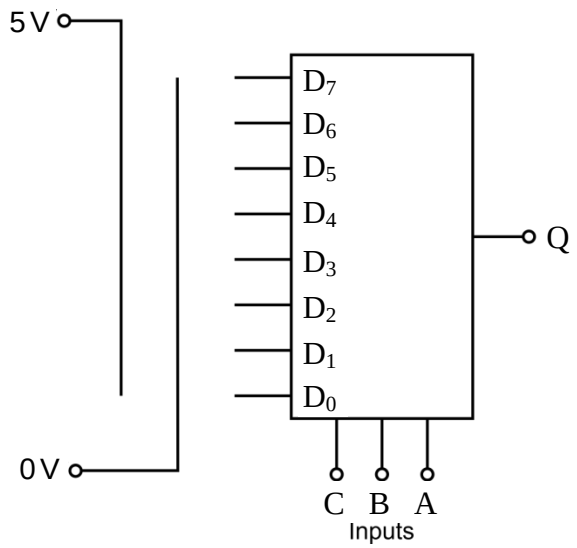
(c) Design a system using a multiplexer IC to generate the following Boolean expression: [5]

$$Q = C.B.\bar{A} + \bar{C}.\bar{B}. + C.A$$

by:

- drawing a truth table for the system;
- completing the circuit diagram.



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3. *(a)* Give **two** characteristics of an **ideal** op-amp. [2]

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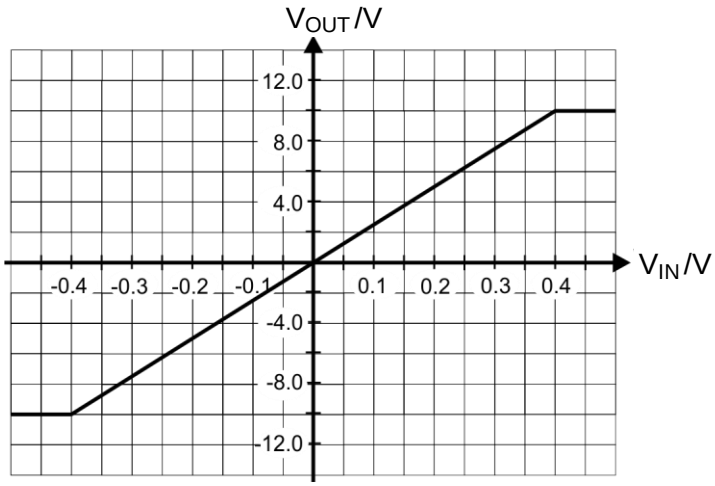
(b) The graph shows the voltage characteristics of an amplifier configured from a practical op-amp.



(i) Determine the biggest input signal amplitude which avoids saturating the output of this amplifier. [2]

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(ii) Calculate the voltage gain of the amplifier. [2]

voltage gain = ...

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(iii) Design the amplifier based on a single op-amp and draw a labelled diagram of your design. [4]

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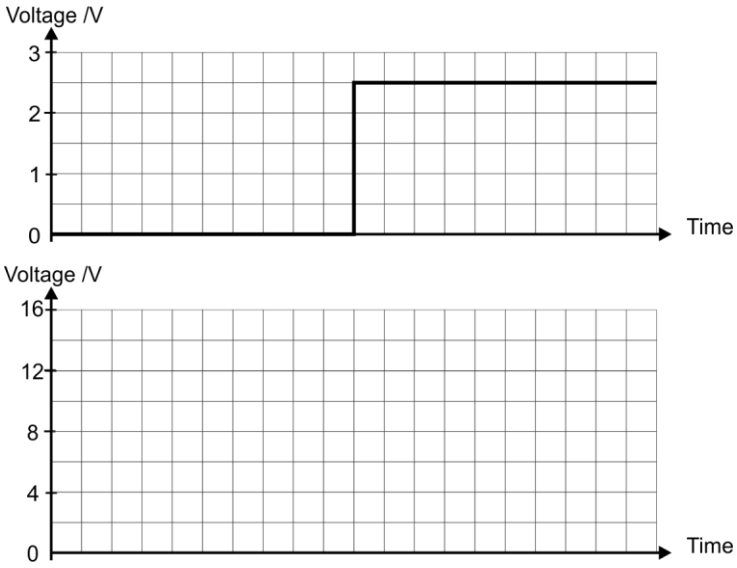
(c) The table gives information about the op-amp used in this circuit.

Characteristic	**Value**
Open-loop gain	1.0×10^6
Input impedance	$5.0 \times 10^6\ \Omega$
Gain bandwidth product	5 MHz
Slew rate	3 V/ μs

The signal shown below is applied to the input of the amplifier.



(i) Calculate the time taken for the output to reach the saturation voltage. [2]

time = ... μs

(ii) **Use the axes provided above** to sketch the output signal. Label your graph with any significant times. [2]

(iii) For a sine wave signal with a peak output voltage of 8 V, calculate the maximum frequency before slew-rate distortion appears. [3]

frequency = ... kHz

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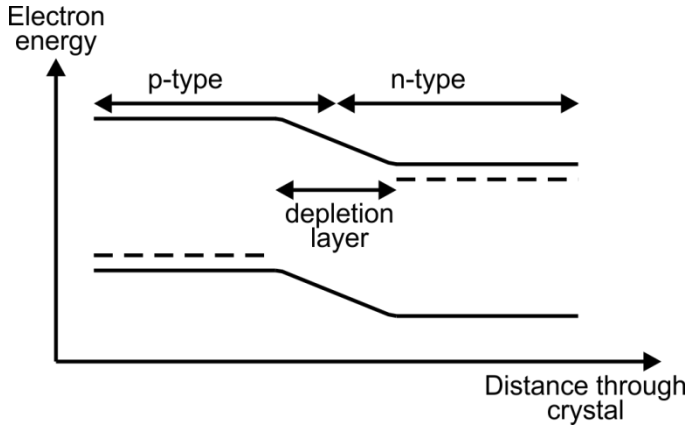
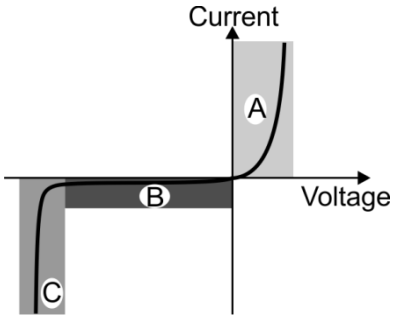
4. *(a)* The energy band structure of a p-n junction is shown in the diagram.



The next diagram shows the I-V characteristics of a silicon diode.



Use the energy band diagram to explain the features labelled A, B and C in the characteristic curve. [4]

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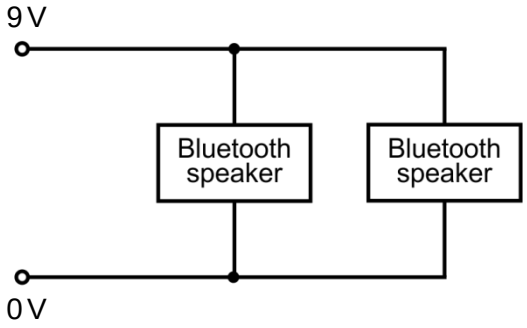
(b) A student wishes to run two Bluetooth speakers from the same battery while providing protection against an incorrect battery connection.

Modify the circuit diagram for this system by adding a single electronic component to provide this reverse voltage protection. [2]



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5. *(a)* (i) Noise and distortion are two undesirable effects in a communications system. Distinguish between the terms 'noise' and 'distortion'. [2]

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(ii) A communications link offers a signal-to-noise ratio of 20 dB. The mean noise power is 0.1 mW. Calculate the mean signal power. [2]

signal power = ... mW

(b) The graph shows a sinusoidal carrier C**,** modulated with a sinusoidal signal, S.

On the graph below, draw the signal S. [2]

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(c) A 200 MHz carrier is frequency modulated by an audio signal with a frequency range of 100 Hz to 20 kHz. The frequency deviation is 100 kHz.

For the resulting FM signal, calculate:

(i) the modulation index; [2]

modulation index = ...

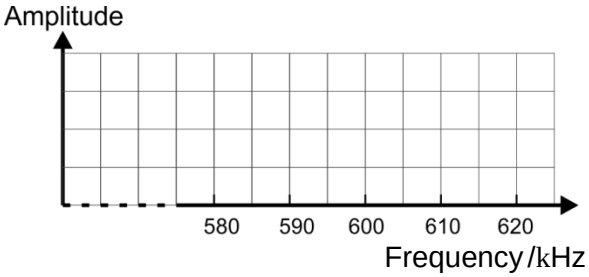
(ii) the bandwidth. [2]

bandwidth = ... kHz

(d) A communications system multiplexes a number of radio broadcasts onto one link. It has an available bandwidth of 2 000 kHz and uses a carrier separation of 10 kHz.

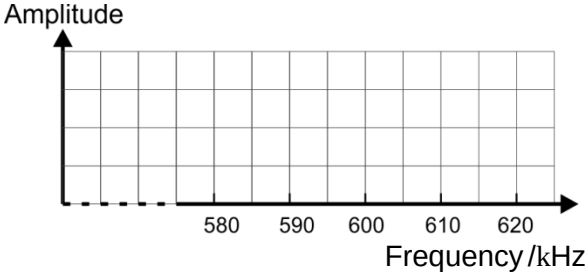
(i) Radio station **P** transmits on a 600 kHz sinusoidal carrier wave. It is **amplitude** modulated by the audio signal which has a frequency range of 0 Hz - 4 kHz.

On the axes below, draw the frequency spectrum of the transmitted wave. [3]



(ii) Radio station **Q** broadcasts in the next available channel above the one used by station **P**. It is also **amplitude** modulated by an audio signal with a frequency range of 0 Hz – 4 kHz.

On the axes below, draw the frequency spectrum for stations **P** and **Q** and add labels to identify each. [2]



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(iii) State how many radio stations, configured like this, can be incorporated into the communications system. [1]

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(e) Multiplexing is used in optical communications systems, where light beams of different wavelengths are combined and transmitted through an optical fibre.

Explain one advantage of using a monomode optical fibre as the communications link in communications systems. [2]

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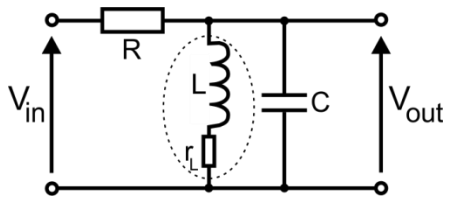
6. One section of an audio system uses a band pass passive filter to limit the frequencies applied to a mid-range loudspeaker.

(a) The output of the amplifier driving the loudspeaker delivers a sinusoidal output with a rms voltage of 10 V.

Calculate the peak voltage of this signal. [2]

peak voltage = ... V

(b) The circuit diagram for the filter is given below.



(i) The filter uses a 68 mH inductor, L, and a 0.33 μF capacitor, C. Determine the frequency at which the output voltage, V_{out}, has its maximum value. [3]

frequency = ... Hz

(ii) Calculate the reactance of the inductor at the filter's resonant frequency. [2]

reactance = ... Ω

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(iii) R is a 680 Ω resistor. The inductor has a DC resistance, r_L, of 25 Ω.

I Calculate the rms value of V_{out} at the resonant frequency. [4]

rms value of V_{out} = ... V

II Calculate the Q factor and bandwidth of its frequency response. [4]

Q factor = ...

bandwidth = ... Hz

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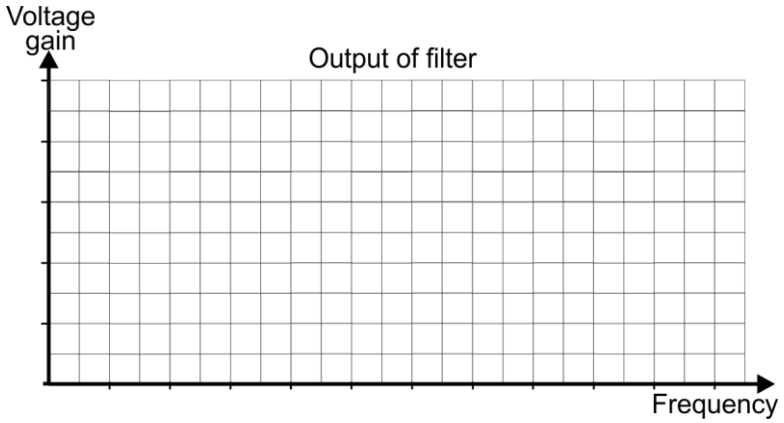
(c) Use the axes provided to sketch a graph of the frequency response of this filter. Add labels to identify the resonant frequency and bandwidth. [3]



(d) When the filter is connected to the speaker system, the resonant frequency is affected by the impedance of the speakers. To correct this, a buffer in the form of an op-amp voltage follower is connected to the output of the filter.

(i) Draw the circuit diagram for the voltage follower using an op-amp. [2]

(ii) Explain why the properties of the voltage follower sub-system overcome the problem described above. [2]

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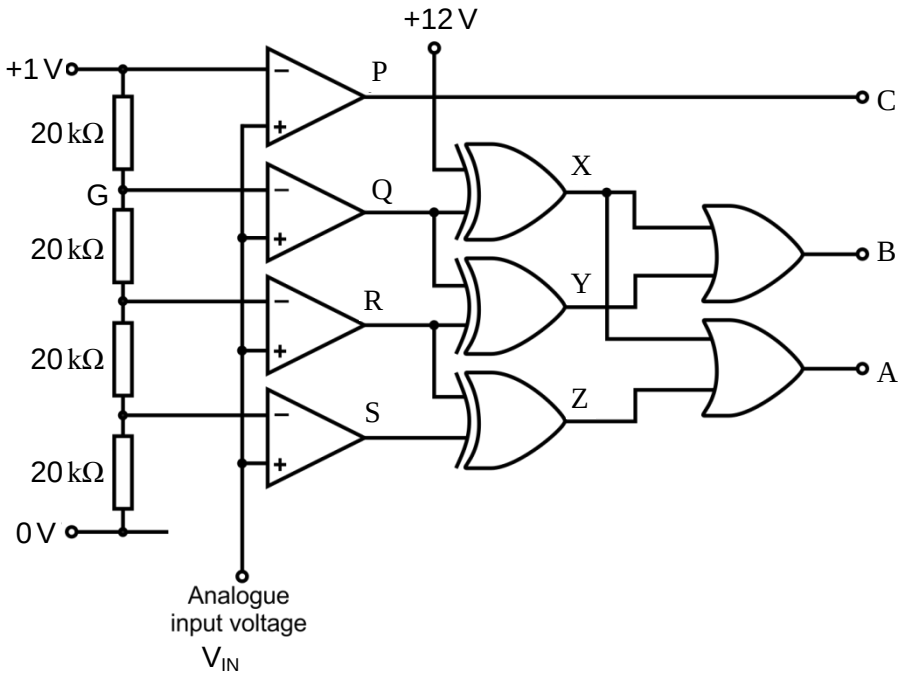
7. The diagram shows the circuit of a flash analogue to digital converter (ADC).



(a) (i) Evaluate the use of this type of Flash ADC compared to a digital ramp ADC. [2]

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(ii) State the purpose of output C. [1]

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(b) Calculate the voltage at point G. [2]

voltage = ... V

(c) Calculate the resolution of this ADC. [2]

resolution = ... V

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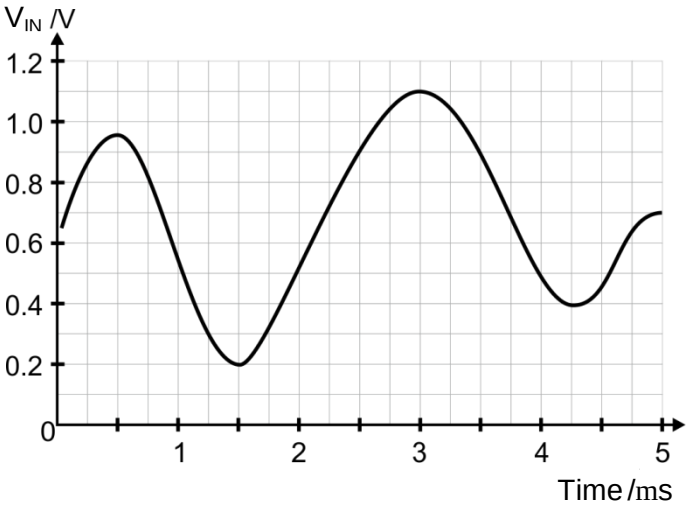
(d) The following signal is applied to the input of the ADC.



(i) The comparator output saturate at +12 V and 0 V.
The system recognises +12 V as logic 1 and 0 V as logic 0.

Complete the table to show:

- the voltages at P, Q, R and S;
- the logic levels at X, Y, Z;
- the logic signals appearing at outputs A, B and C; at the times shown. [4]

Time /ms	**P /V**	**Q /V**	**R /V**	**S /V**	**X**	**Y**	**Z**	**C**	**B**	**A**
1.5										
3.0										
4.5										

(ii) The highest frequency component of the audio signal has a frequency of 12 kHz.

Determine the lowest sampling frequency that allows this signal to be sampled accurately. [1]

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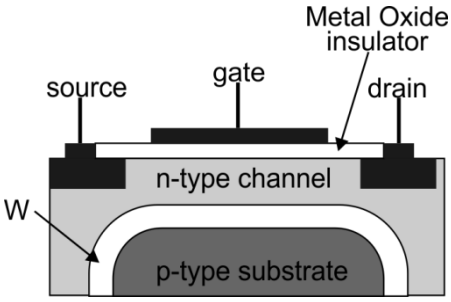
8. *(a)* The following diagram represents the structure of a MOSFET transistor.



The n-type channel is separated from the p-type substrate by a region, labelled W, which contains virtually no free charge carriers.

(i) Name the layer W and the majority free charge carrier in the p-type substrate. [2]

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(ii) Describe and explain changes in the resistance of the n-type channel when a positive voltage is applied to the gate terminal. [3]

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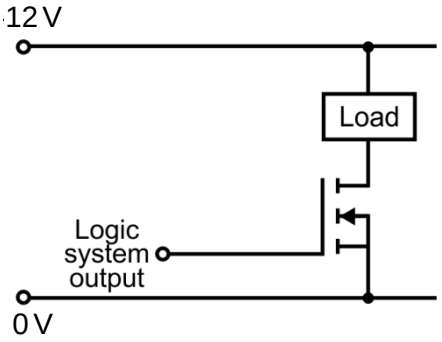
(b) The circuit diagram shows a MOSFET interfacing a logic system to a high-power load.



- The logic level 1 output voltage from the logic system is 10 V.
- For the MOSFET, r_{DSon} = 0.2 Ω

The load current is15 A.

(i) Calculate the minimum value of transconductance g_M. [2]

g_M = ... S

(ii) **Estimate** the gate current. [1]

current = ... A

(iii) Calculate the power dissipated in the MOSFET. [2]

power = ... W

(iv) Calculate the power dissipated in the load. [3]

power = ... W

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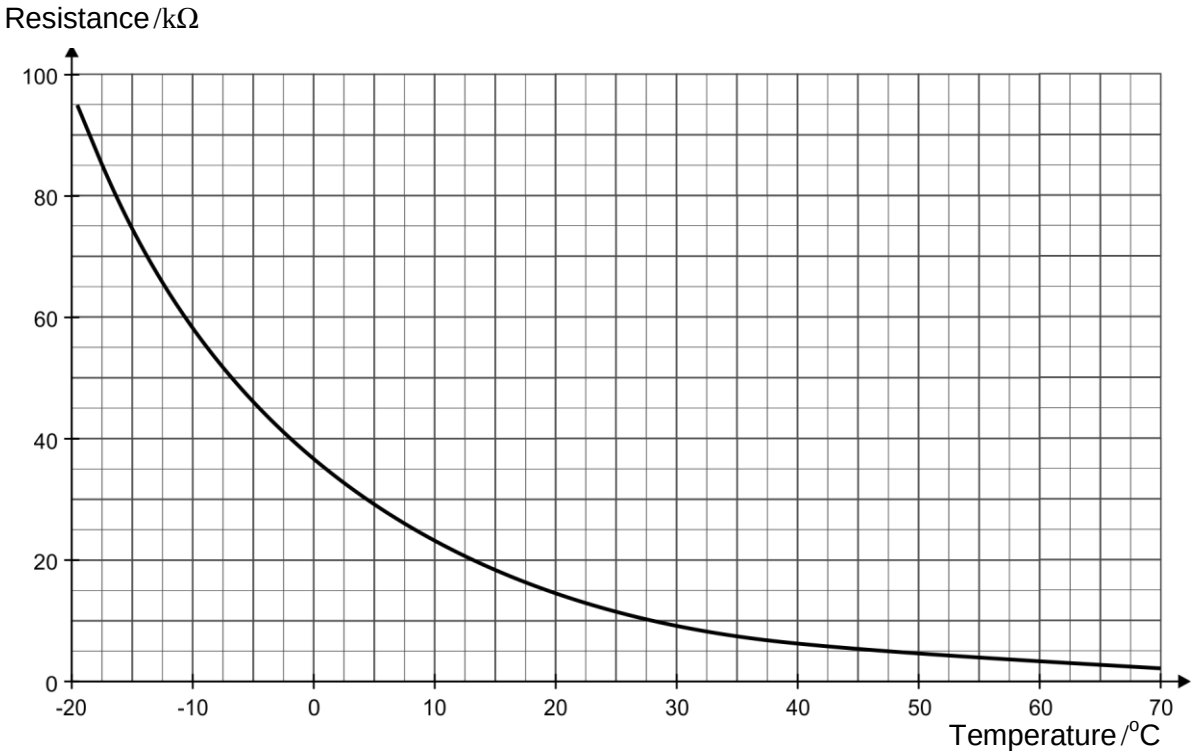
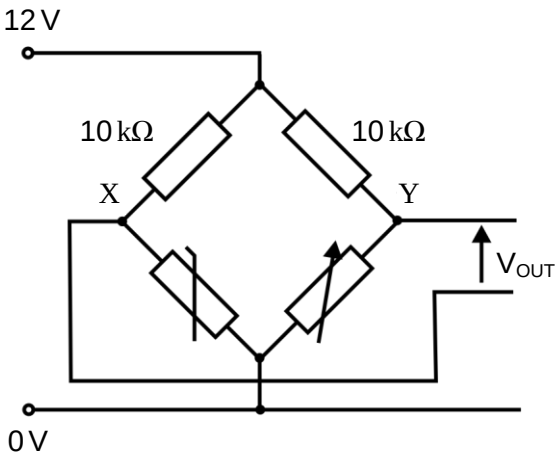
9. *(a)* The thermistor in a temperature meter has the characteristics shown by the following graph.



It is connected in the bridge circuit shown below.



The variable resistor is set to a resistance of 12 kΩ.

(i) Estimate the temperature of the thermistor when the bridge is 'balanced'. Explain how you arrived at your answer. [3]

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(ii) Calculate V_{OUT} when the temperature of the thermistor is 27.5 °C. [4]

V_{OUT} = ... V

(b) Design a difference amplifier, based on an op-amp, to increase the sensitivity of the meter. It has the following properties:

- voltage gain = 50;
- output voltage increases when the temperature increases.

Justify the values chosen for any resistors used in the design. [4]

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10. *(a)* Describe how to measure the frequency response of a passive filter. [3]

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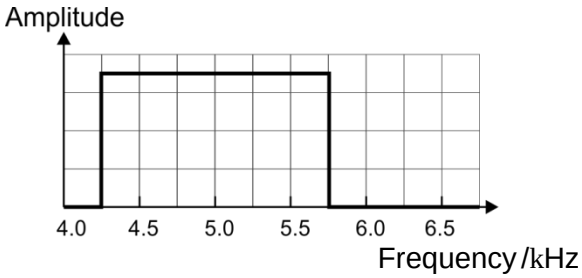
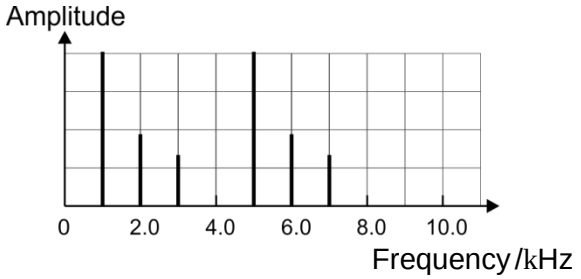
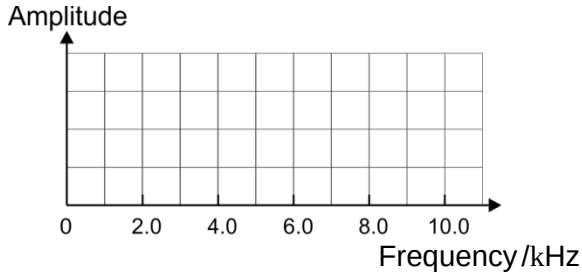
(b) A filter has the characteristic response shown below.



A signal having the following frequency response is applied to the input.



(i) Draw the frequency response of the resulting output signal. [2]



(ii) Use the axes below to sketch two cycles of the resulting signal waveform. Label significant times. [3]

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11. A hearing impaired person wants a system to warn when either the front doorbell switch is pressed or the switch on the back door is pressed.

The LED will flash at a frequency of 1 Hz when the front door switch is pressed and 0.5 Hz when the back door switch is pressed.

(a) Design a suitable logic system for the doorbell warning system and evaluate your chosen design. [6 QER]

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(b) The system incorporates a pulse generator, using a 47 μF capacitor. Unfortunately, this makes the LED flash too slowly. A value around 40 μF is needed.

Design and draw a combination of any of the following four capacitors:

- a 100 μF capacitor,
- a 68 μF capacitor,
- a 47 μF capacitor
- a 22 μF capacitor

to achieve a capacitance close to 40 μF and evaluate your answer. [4]

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END OF PAPER

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A LEVEL ELECTRONICS

COMPONENT 1 – Principles of Electronics – SAMPLE ASSESSMENT MATERIAL

MARK SCHEME

GENERAL INSTRUCTIONS

Recording of marks

Examiners must mark in red ink.

One tick must equate to one mark (except for the extended response question).

Question totals should be written in the box at the end of the question.

Question totals should be entered onto the grid on the front cover and these should be added to give the script total for each candidate.

Marking rules

All work should be seen to have been marked.

Marking schemes will indicate when explicit working is deemed to be a necessary part of a correct answer.

Crossed out responses not replaced should be marked.

Credit will be given for correct and relevant alternative responses which are not recorded in the mark scheme.

Extended response question

A level of response mark scheme is used. Before applying the mark scheme please read through the whole answer from start to finish. Firstly, decide which level descriptor matches best with the candidate's response: remember that you should be considering the overall quality of the response. Then decide which mark to award within the level. Award the higher mark in the level if there is a good match with both the content statements and the communication statement.

Marking abbreviations

The following may be used in marking schemes or in the marking of scripts to indicate reasons for the marks awarded.

cao = correct answer only
ecf = error carried forward

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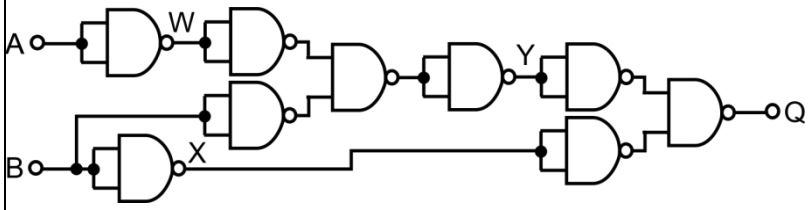
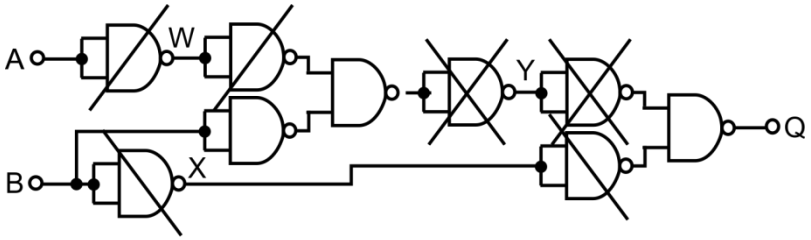
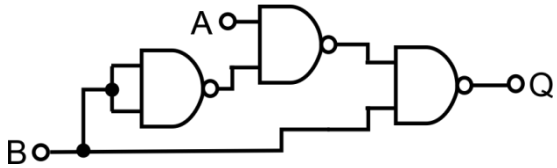
Question		Marking details	Marks available				
			AO1	AO2	AO3	Total	Maths
1	*a*	$X = \overline{B}$ (1) $Y = \overline{\overline{A}+B}$ (1) $Q = \overline{B} + \overline{\overline{A}+B}$ (1)		3		3	3
	b	 Correct replacement for NOT gate (1) Correct replacement for NOR gate (1) Correct replacement for OR gate (1)  All redundant gates identified (1) Redundant gates correctly paired (1)  Correctly redrawn (1)	6			6	
		Question 1 total	**6**	**3**	**0**	**9**	**3**

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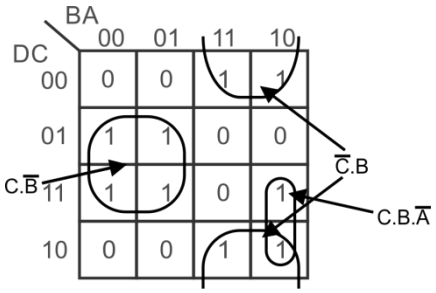
Question			Marking details	Marks available				Maths
				AO1	AO2	AO3	Total	
2	*a*		$Q = \overline{\overline{(A + B)} + C}$ $= (A + B) \cdot \overline{C}$ Alternative $Q = A\,\overline{C} + B.\overline{C}$ Invert the variables (1) Change the sign (1) C B A Q 0 0 0 0 0 0 1 1 ← (1) 0 1 0 1 ← (1) 0 1 1 1 ← (1) 1 0 0 0 1 0 1 0 1 1 0 0 1 1 1 0 Allow **ecf** from simplification Don't accept any additional '1's in the Q column	1 1	1 1 1		5	5
	b		 Each group correctly identified = 1 mark (x3) $Q = C.\overline{B} + \overline{C}.B + C.B.\overline{A}$ Correct expression combining groups (1)		4		4	4

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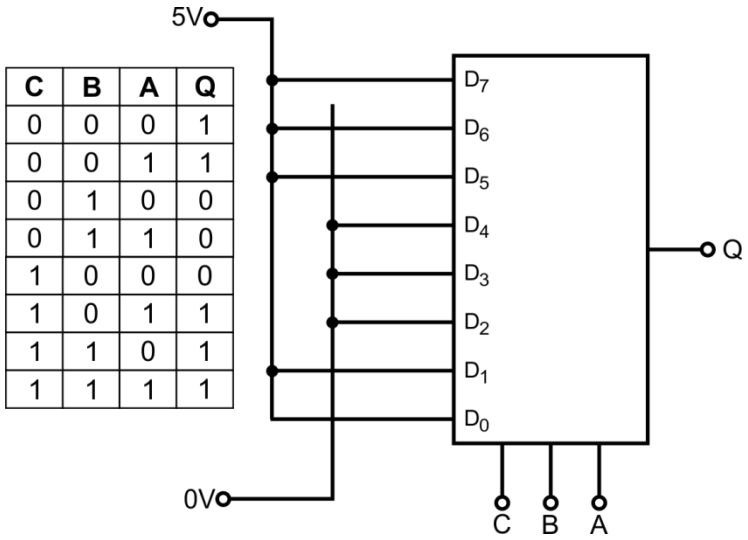
Question			Marking details	Marks available				Maths
				AO1	AO2	AO3	Total	
	c		 C B A Q: 0 0 0 1; 0 0 1 1; 0 1 0 0; 0 1 1 0; 1 0 0 0; 1 0 1 1; 1 1 0 1; 1 1 1 1 Table: Multiplexer correct for C column (1) Multiplexer correct for B column (1) Multiplexer correct for A column (1) Circuit diagram: Correct transfer from table Correct 5 V connections (1) Correct 0 V connections (1)		1 1 1	 1 1	 5	3
			Question 2 total	**2**	**10**	**2**	**14**	**12**

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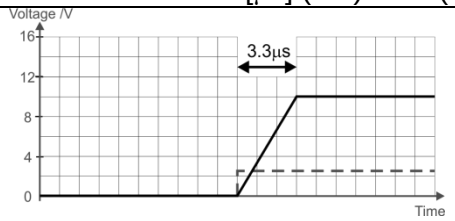
Question			Marking details	Marks available				
				AO1	AO2	AO3	Total	Maths
3	*a*		Any 2 ×(1) from : • infinite open loop gain; • infinite input impedance; • infinite bandwidth; • zero output impedance.	2			2	
	b	i	Recognition of saturation voltage = 10 V (1) Biggest input amplitude (from graph) = 0.4 V (1)	1	1		2	1
		ii	Substitute into $G = \frac{V_{OUT}}{V_{IN}} = \frac{10}{0.4}$ correctly (1) Correct answer = 25 (1)	1	1		2	2
		iii	Correct circuit diagram for an amplifier (1) Non-inverting amplifier (1) Feedback resistor = 24 x R1 (1) All resistors ≥1 kΩ (1)	1	1	1 1	4	1
	c	i	Substitute into $\text{slew rate} = \frac{\Delta V_{OUT}}{\Delta t} = \frac{10}{3}$ correctly (1) Substitution = 3.3 [μs] (**ecf**) from (b)(i) (1)	1	1		2	2
		ii	 Correct shape (1) Appropriate scale with unit on time axis (1) (**ecf**) from (i)		2		2	
		iii	Substitute into correctly $\text{slew rate} = 2\pi f V_P$ (1) $3\times10^6 = 2\pi f \times 8$ Manipulation $f = \frac{3\times10^6}{2\pi\times8}$ (1) Correct answer = 59.7 [kHz] (accept 60 kHz) (1)	1	1 1		3	2
			Question 3 total	**6**	**8**	**3**	**17**	**8**

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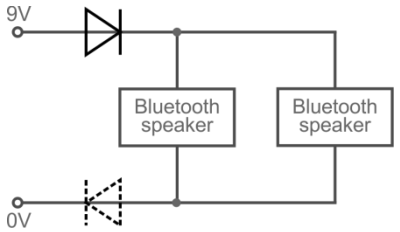
Question			Marking details	Marks available				
				AO1	AO2	AO3	Total	Maths
4	*a*		Recognition of forward and reverse bias (1) A - potential barrier height reduced - easier for charge carriers to flow across junction / electrons attracted to 'p' region and holes to 'n' (1) B - potential barrier height raised - much more difficult for charge carriers to flow across junction / electrons attracted to 'n' region and holes to 'p' (1) C - charge carriers flow to create current - electric field strong enough to create electron-hole pairs throughout depletion region / collisions cause more e/h/ pairs - electrons 'tunnel' through depletion region barrier (1)	4			4	
	b		 Diode correctly selected with symbol AND polarity [1] Correct position to protect both speakers [1] (Alternative shown in dotted lines.)		2		2	
			Question 4 total	**4**	**2**	**0**	**6**	**0**

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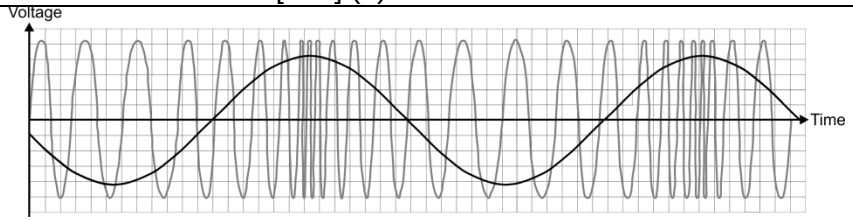
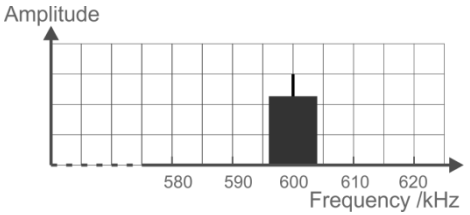
Question			Marking details	Marks available				
				AO1	AO2	AO3	Total	Maths
5	*a*	i	Noise - unwanted external component added to signal (1) Distortion - unwanted additions to frequency spectrum caused by non-linearity of system itself (1)	2			2	
		ii	Substitute and manipulate correctly $\mathrm{SNR}_{\mathrm{dB}} = 10\log_{10}\frac{P_S}{P_N}$ (1) $20 = 10\log_{10}\frac{P_S}{0.1}$ Correct answer = 10[mW] (1)		2		2	2
	b		 Correct period (1) Correct phase (1)		2		2	2
	c	i	Substitute into $\beta = \frac{\Delta f_c}{f_i}$ correctly (1) Correct answer = 5 (1)	1	1		2	2
		ii	Substitute into correctly $\mathrm{Bandwidth} = 2(1+\beta)f_i = 2(1+5)20$ (1) Correct answer = 240 [kHz] (1)	1	1		2	2
	d	i	 Correct shape (1) Correct carrier freq. 600 kHz (1) Correct bandwidth 596 - 604 kHz (1)	1 1	1		3	

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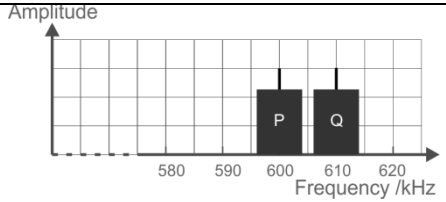
Question			Marking details		Marks available			
				AO1	AO2	AO3	Total	Maths
		ii	 Correct carrier freq. 610 kHz (1) Correct bandwidth 606 - 614 kHz (1)	1	1		2	
		iii	200 channels		1		1	1
	e		Fibre optic cable has enormous bandwidth (1) Bigger bandwidth means more channels can be multiplexed (1) **Alternative** Fibre optic cable immune from electromagnetic interference (1) Can be used in electrically noisy locations (1) **Alternative** Not electrical (1) Can be used between buildings having different earth potentials (1) **Alternative** Low attenuation losses (1) Fewer repeater stations needed (1)	2			2	
			Question 5 total	**9**	**9**	**0**	**18**	**9**

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Question			Marking details	Marks available				
				AO1	AO2	AO3	Total	Maths
6	*a*		Substitute and manipulate $V_{rms} = \frac{V_0}{\sqrt{2}}$ $V_0 = 10 \times \sqrt{2}$ (1) Correct answer = 14 V (accept 14.1 V and 14.14 V) (1)		2		2	2
	b	i	Max output voltage at resonant frequency (or implied) (1) Substitute into $f_0 = \frac{1}{2\pi\sqrt{L\,C}} = \frac{1}{2\pi\sqrt{68\times10^{-3}\times0.33\times10^{-6}}}$ (1) Correct answer = 1062.5 [Hz] (accept 1063 Hz or 1.06k Hz) (1)	1 1	 1		 3	 2
		ii	Substitute into $X_L = 2\pi fL = 2\pi 1062.5 \times 68 \times 10^{-3}$ correctly (1) Correct answer = 454 [Ω] (accept 0.454 kΩ) (1)	1	 1		 2	 2
		iii I	Substitute into $R_D = \frac{L}{r_L C} = \frac{68\times10^{-3}}{25\times0.33\times10^{-6}}$ correctly (1) Correct answer = 8242 [Ω] (1) Substitute result in $V_{OUT} = \frac{R_2}{R_1 + R_2} V_{IN} = \frac{8242}{680 + 8242} \times 10$ (1) Correct answer = 9.24 [V] (accept 9.2 V) (1)	1 1	 1 1		 4	 4
		II	Substitute into $Q = \frac{2\pi\, f_0\, L}{r_L} = \frac{2\pi \times 1062.5 \times 68 \times 10^{-3}}{r_L}$ (1) Q = 18.2 (allow **ecf** from (b)) (1) Substitute and re-arrange $Q = \frac{f_0}{\text{bandwidth}}$ $\text{bandwidth} = \frac{f_0}{Q} = \frac{1062.5}{18.2}$ (1) Bandwidth = 58.5 [Hz] (allow **ecf** from Q answer) (1)	1	 1 1 1		 4	 4

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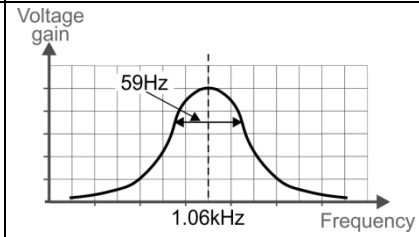
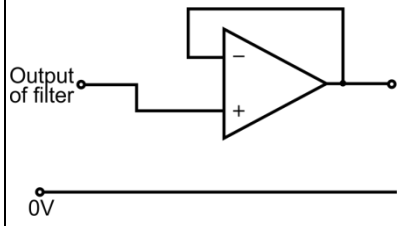
Question			Marking details	Marks available				
				AO1	AO2	AO3	Total	Maths
	c		 Correct shape (1) Correct bandwidth (1) Correct resonant freq (1)	1	1 1		3	
	d	i	 Negative feedback loop correct (1) Input signal to non-inv. input (1)	2			2	
		ii	Input impedance is very high (1) Does not load the filter / affect the break frequency / have any effect on the resistance of the filter. (1)	1	1		2	
			Question 6 total	**10**	**12**	**0**	**22**	**14**

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<table>
<tr><th colspan="3" rowspan="2">Question</th><th rowspan="2">Marking details</th><th colspan="4">Marks available</th><th></th></tr>
<tr><th>AO1</th><th>AO2</th><th>AO3</th><th>Total</th><th>Maths</th></tr>
<tr><td>7</td><td>a</td><td>i</td><td>Evaluations should refer to:
shorter conversion time using flash ADCs (1)
but have a more complex circuit / expensive to achieve the same function (1)</td><td></td><td></td><td>2</td><td>2</td><td></td></tr>
<tr><td></td><td></td><td>ii</td><td>To indicate that input voltage exceeds conversion voltage range</td><td>1</td><td></td><td></td><td>1</td><td></td></tr>
<tr><td></td><td>b</td><td></td><td>Substitute into $V_{OUT} = \frac{R_2}{R_1 + R_2} V_{IN} = \frac{60}{20+60} \times 1$ correctly (1)
Voltage at G = 0.75 [V] (1)</td><td>1</td><td>1</td><td></td><td>2</td><td>2</td></tr>
<tr><td></td><td>c</td><td></td><td>Substitute into $\text{resolution} = \frac{\text{i/p voltage range}}{2^n} = \frac{1}{2^2}$ correctly (1)
Correct answer = 0.25 [V] (1)</td><td>1</td><td>1</td><td></td><td>2</td><td>2</td></tr>
<tr><td></td><td>d</td><td>i</td><td>
<table>
<tr><th>Time</th><th>P</th><th>Q</th><th>R</th><th>S</th><th>X</th><th>Y</th><th>Z</th><th>C</th><th>B</th><th>A</th></tr>
<tr><td>1.5</td><td>12</td><td>12</td><td>12</td><td>12</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td></tr>
<tr><td>3.0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td></tr>
<tr><td>4.5</td><td>12</td><td>12</td><td>12</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td><td>1</td></tr>
</table>
All comparator outputs correct (1)
Correct signals at X, Y and Z (1)
Outputs B and A correct (1)
Correct behaviour of output C (1)</td><td></td><td>4</td><td></td><td>4</td><td>4</td></tr>
<tr><td></td><td></td><td>ii</td><td>Use of Nyquist’s theorem to give 24 kHz</td><td></td><td>1</td><td></td><td>1</td><td></td></tr>
<tr><td></td><td></td><td></td><td>Question 7 total</td><td>5</td><td>7</td><td>0</td><td>12</td><td>8</td></tr>
</table>

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Question			Marking details	Marks available				
				AO1	AO2	AO3	Total	Maths
8	*a*	i	W = depletion layer (1) Majority carrier in p-type = holes (1)	2			2	
		ii	Initially few free charges in channel so high resistance (1) Electrons from substrate attracted to region beneath gate terminal (i.e. the channel) (1) Channel resistance falls (1)	3			3	
	b	i	Substitute and manipulate correctly $I_D = g_M(V_{GS} - 3)$ $g_M = \frac{15}{10-3}$ (1) Correct answer = 2.14 [S] (1)		2		2	2
		ii	Gate current = 0	1			1	
		iii	Substitute into $P = I^2R = 15^2 \times 0.2$ correctly (1) Correct answer = 45 [W] (1)	1	1		2	2
		iv	Voltage across load = 12 - (15 x 0.2) = 9 [V] (1) Substitute into $P = VI = 9 \times 15$ correctly (1) Correct answer = 135 [W] (1)	1	1 1		3	3
			Question 8 total	**8**	**5**	**0**	**13**	**7**

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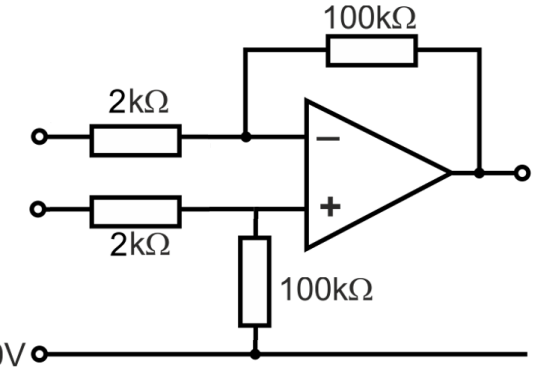
Question			Marking details	Marks available				
				AO1	AO2	AO3	Total	Maths
9	*a*	i	Bridge balanced when voltage at X = voltage at Y. (1) For this, ratio of resistors on either side must be the same. Thermistor resistance = variable resistor resistance = 12 kΩ (1) From graph, this occurs at 25 ℃ (± 2 ℃) (1)	1	1 1		3	1
		ii	At 27.5 ℃, thermistor resistance = 10 kΩ (from graph) (1) Substitute into $V_{OUT} = \frac{R_2}{R_1 + R_2} V_{IN} = \frac{10}{20} \times 12 = 6$ for LH arm (1) Substitute into $V_{OUT} = \frac{R_2}{R_1 + R_2} V_{IN} = \frac{12}{22} \times 12 = 6.55$ for RH arm (1) Correct answer = 0.55 V (accept 0.6 V) (1)		4		4	4
	b		 Inverting input connections correct (1) Non-inverting input connections correct (1) Suitable resistor values ≥ 1 kΩ(ratio of 50) (1) Resistor value choice justified (1)			4	4	1
			Question 9 total	**1**	**6**	**4**	**11**	**6**

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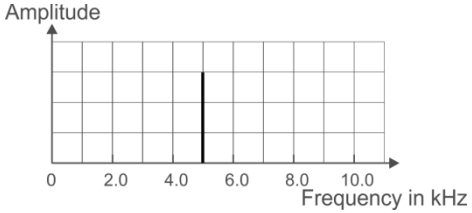
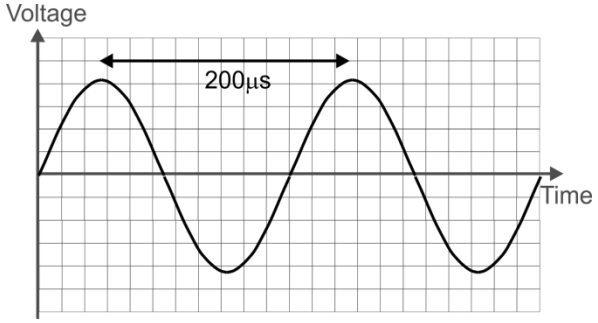
Question			Marking details	Marks available				
				AO1	AO2	AO3	Total	Maths
10	*a*		Use signal generator to generate input signal and oscilloscope to monitor output voltage. (1) Vary frequency of input signal and measure amplitude of output signal. (1) Then (×1) from: calculate voltage gain for each frequency and plot graph of voltage gain vs frequency. or keep input signal at constant amplitude and plot a graph of output amplitude vs frequency.	1		2	3	
	b	i	 Only 1 frequency present (1) 500 Hz component (1)		2		2	
		ii	 Sine wave signal (1) Two cycles (1) Period = 200 μs (1)	1	1 1		3	3
			Question 10 total	**1**	**4**	**3**	**8**	**3**

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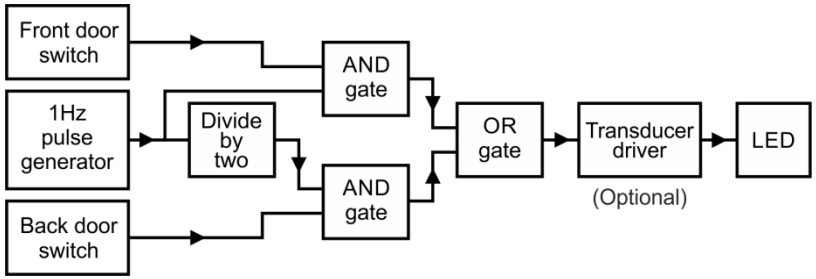
Question			Marking details	Marks available				
				AO1	AO2	AO3	Total	Maths
11	*a*		**Indicative content:**  When the front door switch is pressed, it outputs a logic 1 signal. The upper AND gate then passes 1 Hz pulses from the pulse generator to the OR gate. These pass through the OR gate to the LED, which flashes with a frequency of 1 Hz. The divide-by-two sub-system reduces the frequency of pulses from the pulse generator to 0.5 Hz. It is preferable to a second pulse generator because its output frequency is clamped to be a half of the input frequency. When the back door switch is pressed, it outputs a logic 1 signal. The lower AND gate then passes the 0.5 Hz pulses from the divide-by-two sub-system to the OR gate. These pass through the OR gate to the LED which flashes with a frequency of 0.5 Hz. **AO2** allocation – application of knowledge of role of sub-systems **AO3** allocation – design and evaluation of system **5-6 marks** The block diagram or description of the system is correct. A description of the system's performance is given in terms of the function of each sub-system using logic levels and/or frequencies. An evaluation of the use of the divide-by-two sub-system to a second pulse generator. *There is a sustained line of reasoning which is coherent, substantiated and logically structured. The information included in the response is relevant to the argument.*		2	4	6	

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Question			Marking details	Marks available				
				AO1	AO2	AO3	Total	Maths
			3-4 marks The general structure of the system is correct in a block diagram or description. There is a partial description of the signals, probably without reference to logic levels or frequencies. The divide-by-two sub-system may be replaced by a second pulse generator. *There is a line of reasoning which is partially coherent, supported by some evidence and with some structure. Mainly relevant information is included in the response but there may be some minor errors or the inclusion of some information not relevant to the argument.* **1-2 marks** Three input sub-systems and the output are identified and there is an outline description of their performance. There is recognition of the need for a logic system but only vague statements about its structure. *There is a basic line of reasoning which is not coherent, supported by limited evidence and with very little structure. There may be significant errors or the inclusion of information not relevant to the argument.* **0 marks** *No attempt made or no response worthy of credit.*				6	
	b		Correct use of $\frac{1}{C}=\frac{1}{C_1}+\frac{1}{C_2}$ / $C=\frac{C_1C_2}{C_1+C_2}$ / $C=C_1+C_2$ formulae for combinations (1) Correct results for combinations (1) Correct design of combinations of capacitors (1) Appropriate evaluation including minimum number of capacitors used to achieve value to reduce cost or improve reliability (1)		1 1	1 1	4	2
			Question 11 total	**0**	**4**	**6**	**10**	**2**
			TOTAL	**52**	**70**	**18**	**140**	**72**

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Candidate Name	Centre Number					Candidate Number				

A LEVEL ELECTRONICS

COMPONENT 2

Application of Electronics

SAMPLE ASSESSMENT MATERIAL

2 hours 45 minutes

For Examiner's use only		
Question	**Maximum Mark**	**Mark Awarded**
1.	13	
2.	6	
3.	12	
4.	11	
5.	17	
6.	17	
7.	11	
8.	8	
9.	13	
10.	18	
11.	10	
12.	4	
Total	140	

ADDITIONAL MATERIALS

In addition to this examination paper,
you will require a calculator and a **Data Booklet**.

INSTRUCTIONS TO CANDIDATES

Use black ink or black ball-point pen.
Answer **all** questions.
Write your name, centre number and candidate number in the spaces at the top of this page.
Write your answers in the spaces provided in this booklet.

INFORMATION FOR CANDIDATES

The number of marks is given in brackets at the end of each question or part-question.
The assessment of the quality of extended response (QER) will take place in question **6(d)**.

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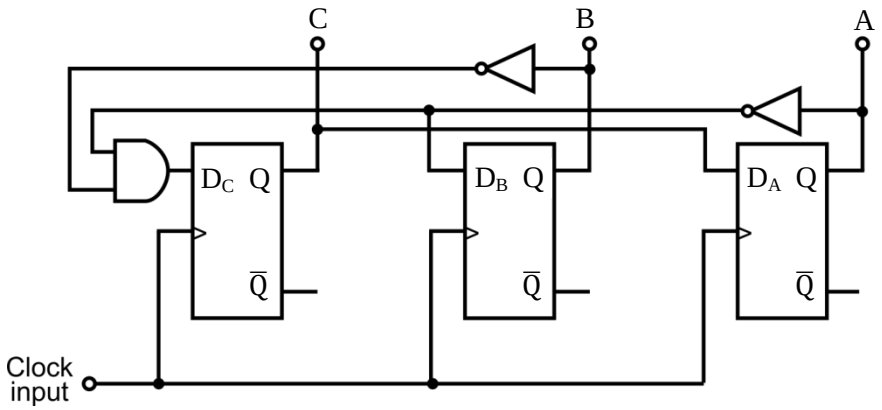
Answer **all** *questions.*

1. A student designs a light-chaser effect, based on a synchronous counter, for a model car.

Part of the circuit diagram is shown below.



(a) Write Boolean expressions for inputs D_A, D_B and D_C in terms of outputs A, B and C. [3]

D_A = …….

D_B = …….

D_C = …….

(b) Use the above expressions to complete the table to show the sequence of output states that the system will generate. You should find only **three** states in the sequence. [2]

State	A	B	C	D_A	D_B	D_C
0	0	0	0			
1						
2				0	0	0

(c) Complete the table below by listing the unused states and determine the state that each unused state progresses to. [3]

	Current Outputs			Next Outputs		
State	A	B	C	A	B	C
3						
4						
5						
6						
7						

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(d) Draw the state diagram for this system. [2]

(e) There is a serious defect with the design of this sequence generator. Identify the defect and the issues associated with it and redesign the system to overcome it without changing the main sequence. [3]

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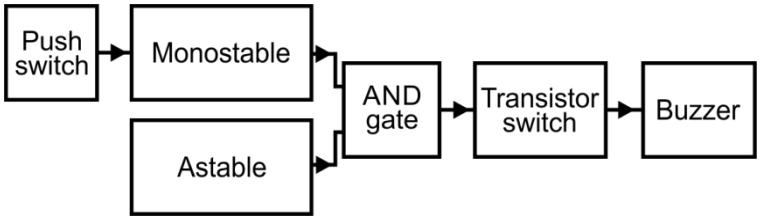
2. The following alarm system sets off a buzzer when the monostable is triggered.



- The monostable output remains at logic 1 for 10 seconds after it is triggered.
- The astable has an equal mark-space ratio and a period of 2 seconds.

(a) The monostable is triggered. Describe the behaviour of the buzzer over the next 15 seconds. [2]

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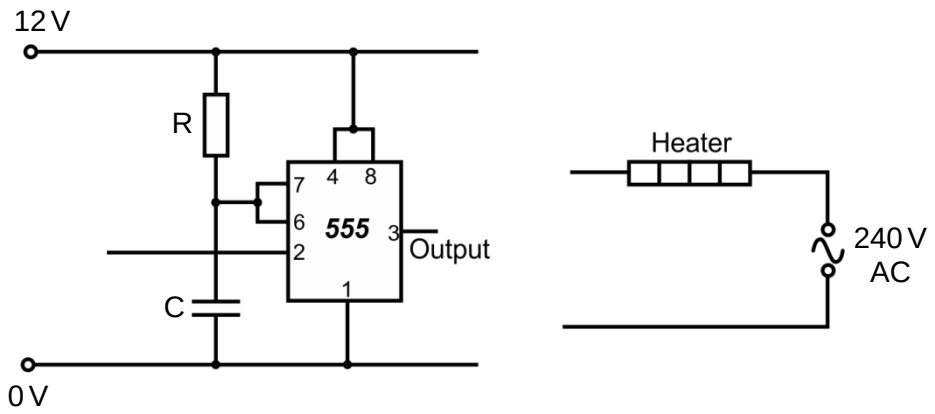
(b) A greenhouse is kept warm by a 240 V AC mains heater. The heater comes on for a predetermined time when a switch is pressed.

The following diagram shows an incomplete circuit for a 555 monostable timer used to control the heater. The 555 is falling-edge triggered. The monostable output is interfaced to the heater by a relay.

Complete the circuit diagram. [4]



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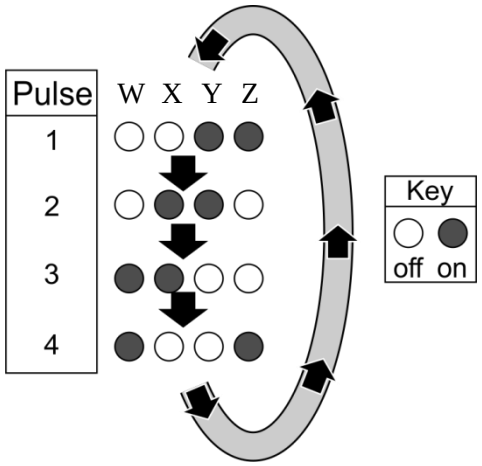
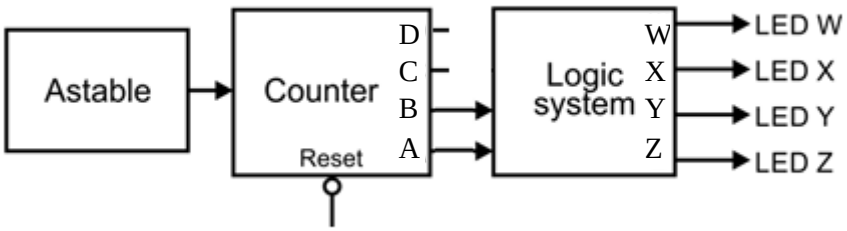
3. A student wants a lighting effect for an electronic game, which contains four LEDs, W, X, Y and Z. These flash in the sequence illustrated in the diagram given below.



The LEDs are controlled by a counter and logic system, controlled by pulses from an astable sub-system as the block diagram shows.



The truth table linking the logic system outputs to the counter outputs is shown below. Each LED lights when it receives a logic 1 signal.

Pulse	**Counter outputs**				**Logic system outputs**			
	D	**C**	**B**	**A**	**W**	**X**	**Y**	**Z**
1	0	0	0	0	0	0	1	1
2	0	0	0	1	0	1	1	0
3	0	0	1	0	1	1	0	0
4	0	0	1	1	1	0	0	1
5	0	1	0	0	Reset			

(a) **Complete the block diagram above** to show how the counter is reset on every fifth pulse. [2]

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(b) Design a logic system to produce the sequence. Your answer should include the Boolean expressions required to justify your design. [8]

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(c) The student finds that the LEDs are too dim and so replaces them with high power LEDs. Each of these requires a buffer between it and the logic system.

Draw the circuit diagram to show how a bipolar transistor switch could be used as the interface between output **W** and a high power LED. [2]

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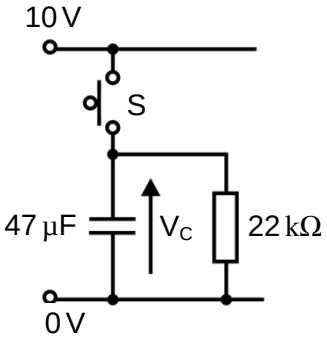
4. *(a)* Pulse generators use RC networks to control signal timing. The diagram shows a RC network.



Switch S is closed and immediately opened at time t = 0.

(i) Calculate the time at which the voltage V_C is 5 V. [2]

time = ... s

(ii) Calculate the time at which the voltage V_C is 8 V. [2]

time = ... s

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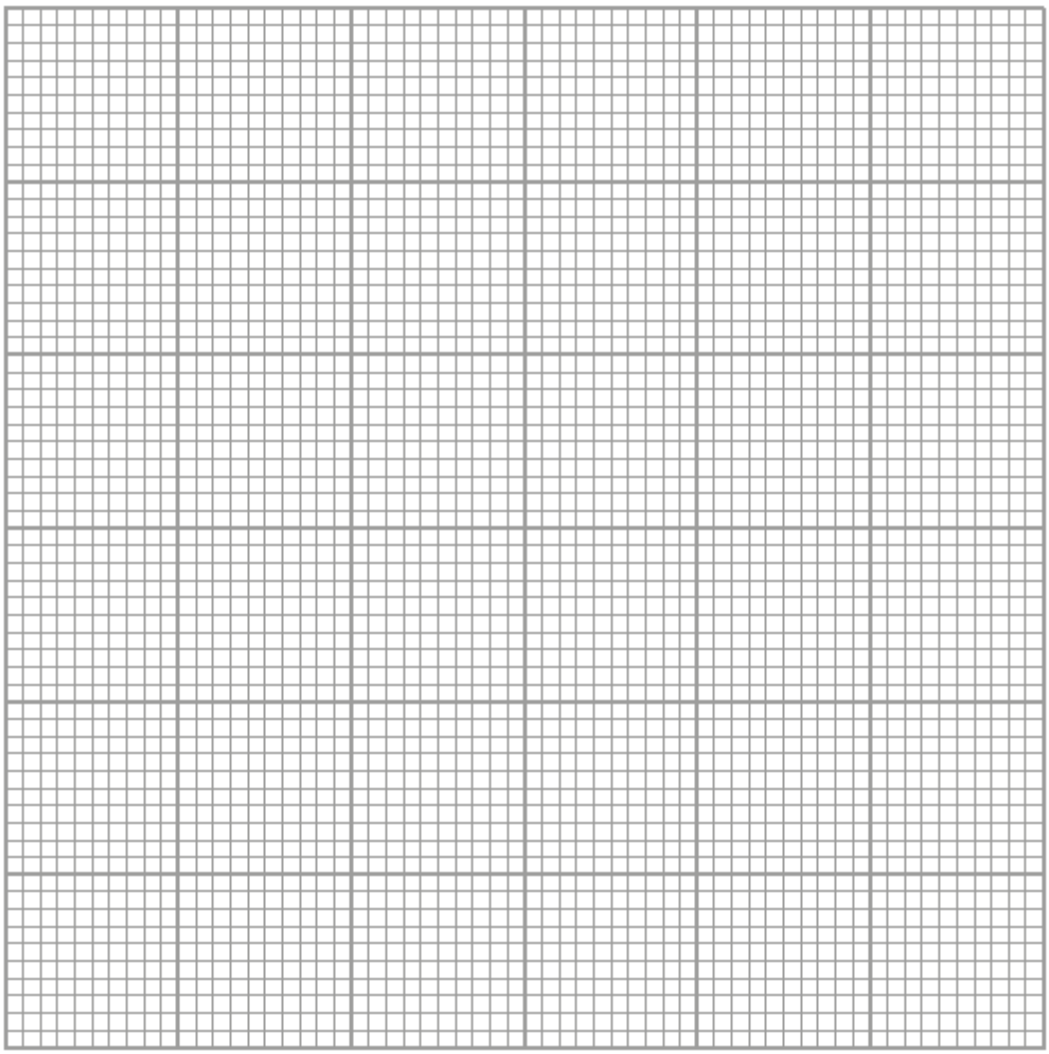
(iii) Draw and label a graph to show what happens to V_C up to a time t = 10 s. [3]



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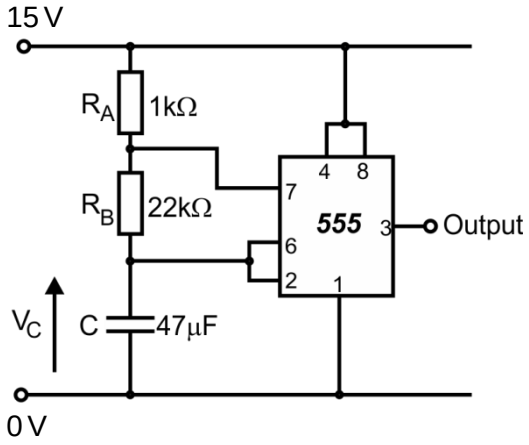
(b) The circuit diagram for an astable based on a 555 IC is shown below.



Calculate:

(i) the mark / space ratio for this astable [2]

mark / space ratio = ...

(ii) the duration of the 'space' for the output waveform. [2]

time = ... s

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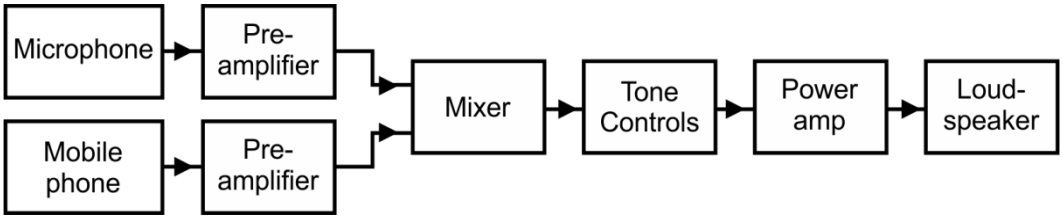
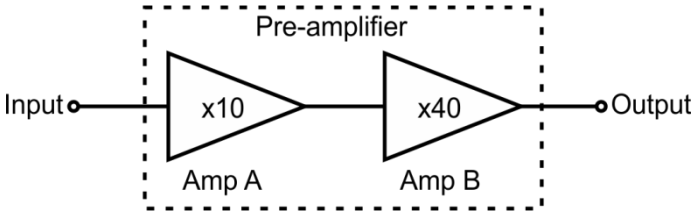
5. The block diagram shows a public address system.



(a) Each pre-amplifier has an overall gain of 400, made by coupling together two non-inverting amplifiers, A and B.



The table gives some data on the op-amps used throughout the public address system.

Parameter	**Typical Value**
Open-loop voltage gain	10^5
Input resistance	$10^{12}\,\Omega$
Gain bandwidth product	$1\,\mathrm{MHz}$
Slew-rate	$9\,\mathrm{V}\,\mu\mathrm{s}^{-1}$
Common mode rejection ratio	$90\,\mathrm{dB}$

Determine the bandwidth of the pre-amplifier and state how can it be increased without changing the overall gain of the pre-amplifier.
(Give new values for the voltage gains of the amplifiers.) [2]

bandwidth = ... kHz

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(b) The mixer allows signals from each source to be faded in or out independently.

Part of the specification for the mixer is given below.

Description	**Value**
Number of input channels	2
Maximum voltage gain on input channels	10
Minimum input impedance (either channel)	10 kΩ
Bandwidth (either channel)	15 kHz

It is based on a summing amplifier using an op-amp with the characteristics given in the table above.

Design a mixer which meets this specification. Include a circuit diagram, and component values for your design. [5]

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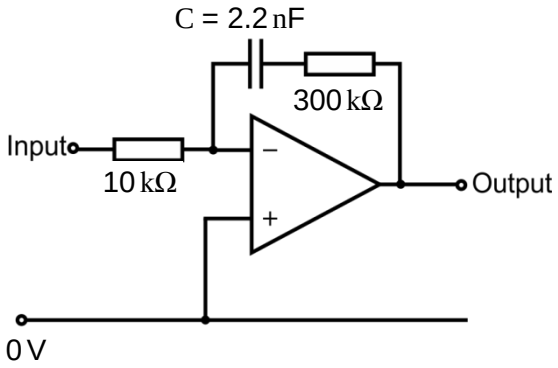
(c) A filter circuit is shown below.



(i) Identify this type of active filter and calculate its break frequency. [4]

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break frequency = ... Hz

(ii) Calculate the voltage gain of the filter at frequencies well above the break frequency. [2]

voltage gain = ...

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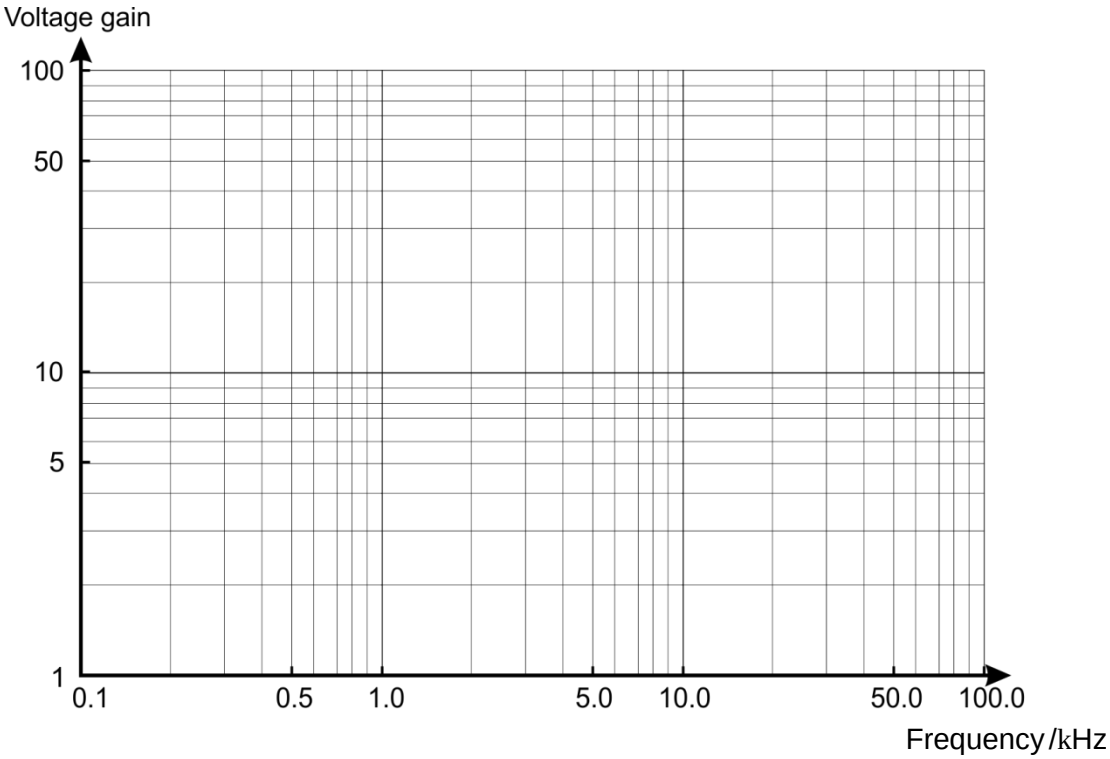
(iii) Use the axes provided to draw the frequency response of this filter. [3]



(iv) State the modification to the circuit required to allow the filter to be used as a tone control. [1]

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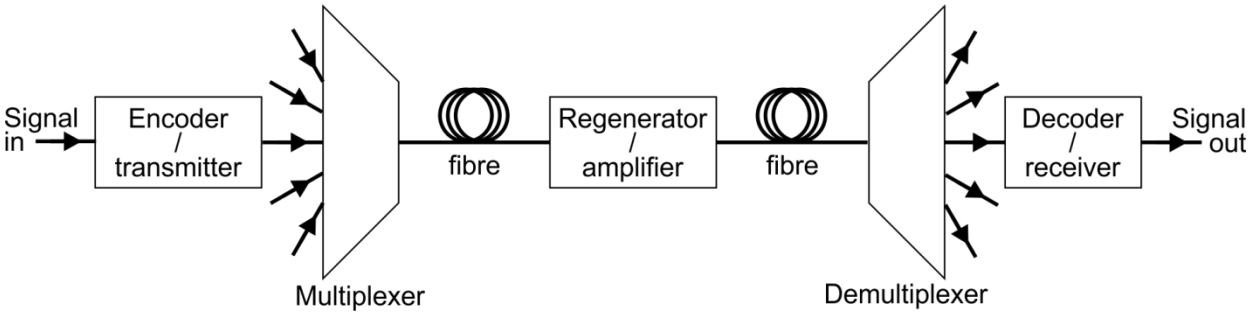
6. The block diagram shows a typical optical communication system.



(a) Two commonly used light sources for the optical signal are LEDs and laser diodes. Give two advantages of a laser diode compared to a LED. [2]

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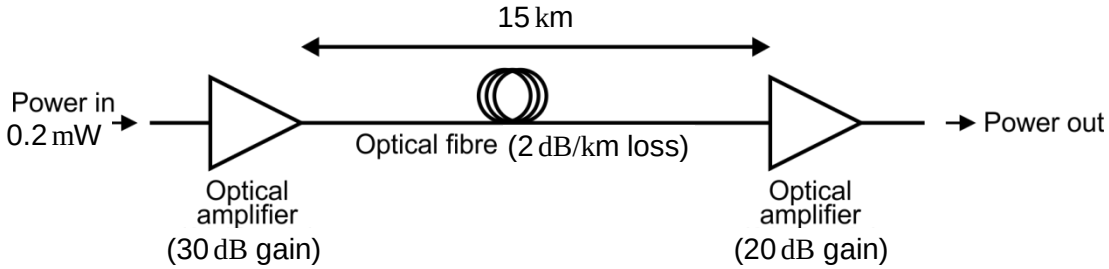
(b) The diagram shows part of an optical communication system. It shows a 15 km length of optical fibre, which has a cable loss of 2 dB/km and two regenerators.



Calculate the power leaving this section of the communication system. [4]

power = ... mW

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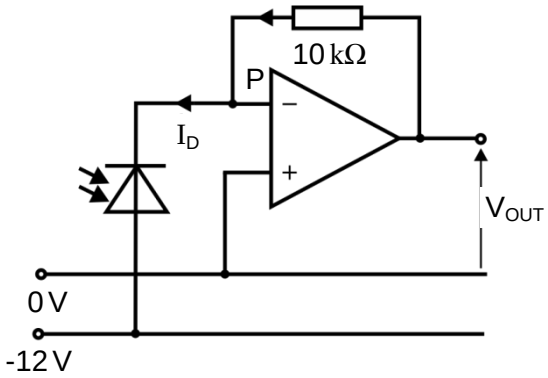
(c) The circuit diagram for a simple optical fibre receiver is given below. It consists of a photodiode and an op-amp configured as a current-to-voltage converter.



(i) Explain why the voltage at point P at the inverting input of the op-amp, is zero providing the op-amp output is not saturated. [2]

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(ii) Explain why the current through the feedback resistor is virtually equal to that through the photodiode. [2]

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(iii) Calculate the output voltage V_{OUT} when the current through the photodiode is 0.25 mA. [1]

V_{OUT} = ... V

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(d) A network engineer is designing a communications network for a university campus.

She has to decide between using multimode and monomode optical fibres for the communications link.

Evaluate the advantages and disadvantages of each for use in this system.
[6 QER]

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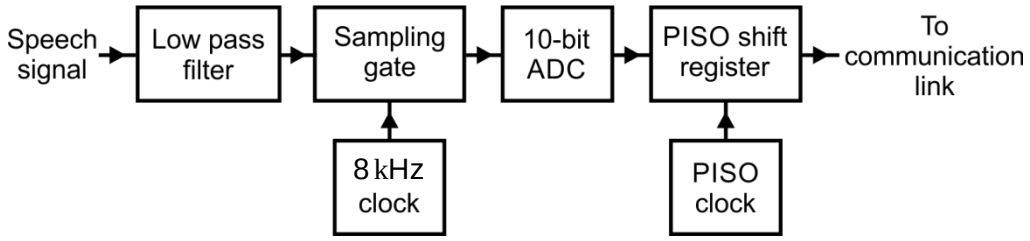
7. The following block diagram shows a *Pulse Code Modulation* (PCM) transmitter used to transmit speech information, in the range 50 Hz to 3.9 kHz, by telephone.



(a) Determine the minimum frequency for the PISO Clock for this PCM transmitter. Justify your answer. [2]

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(b) Draw a block diagram of a suitable PCM receiver. [3]

(c) A Schmitt trigger is used to *regenerate* the signal received down the communication channel.

Here is part of the data sheet for a Schmitt trigger connected to a 10 V power supply:

Characteristic	**Value**
Logic 1	10 V
Logic 0	0 V
1 / 0 threshold for a **rising** voltage	7 V
0 / 1 threshold for a **falling** voltage	3 V

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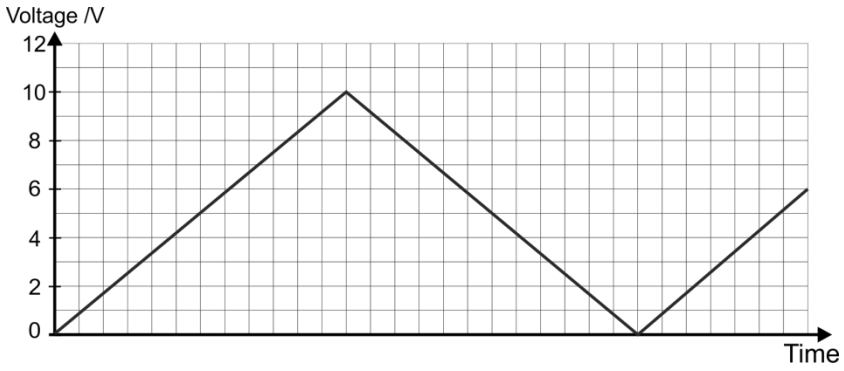
(i) An engineer tests the performance of the Schmitt trigger by inputting the signal shown in the graph.



Draw the corresponding output signal on the graph. [2]

(ii) This Schmitt trigger is used to regenerate the noisy digital signal shown in the next graph.

Draw the output signal from the Schmitt trigger on the graph.
Comment on its performance as a regenerator for this signal. [4]

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8. *(a)* In the specification for a power supply, distinguish between the terms line regulation and load regulation. [2]

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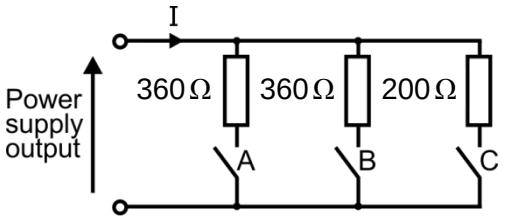
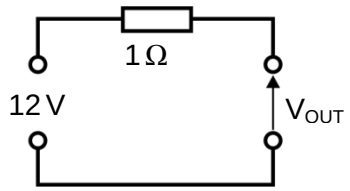
(b) A student uses the following array of resistors to test the performance of a power supply, described as 12 V, 100 mA DC under different loads.



Complete the table to show the total resistance of the array when different combinations of switches are closed. [2]

Switches closed	Total resistance /Ω
A	
A and B	
A and B and C	

(c) The Thevenin equivalent circuit of the power supply is shown below.



(i) Switches A and B are closed. Calculate the V_{OUT} of the power supply. [2]

V_{OUT} = ... V

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(ii) Finally, all three switches are closed. Calculate the V_{OUT} of the power supply. [2]

V_{OUT} = ... V

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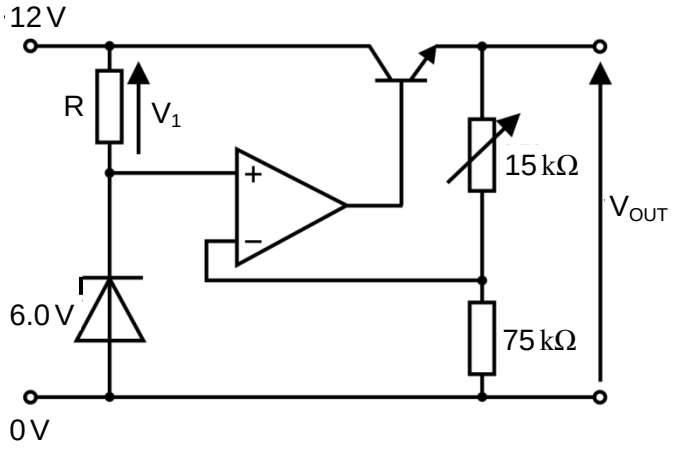
9. Here is part of the circuit diagram for a regulated power supply.
It uses a 6.0 V zener diode.



(a) The zener diode requires a minimum current of 10 mA to maintain it in reverse breakdown. The current flowing into the non-inverting input of the op-amp is insignificantly small. Calculate the maximum resistance of resistor R. [3]

resistance = ... Ω

(b) Calculate the minimum power rating for the zener diode. [2]

power = ... mW

(c) Calculate the power supply output voltage range. [3]

voltage range = ...

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(d) When the variable resistor is set to minimum resistance, the load attached to the output draws a current of 120 mA. The transistor has a current gain, h_{FE}, of 40. Calculate the current delivered by the output of the op-amp. [3]

current = ... mA

(e) The power supply voltage increases from 12 V to 13 V.
Explain why the output voltage remains unchanged. [2]

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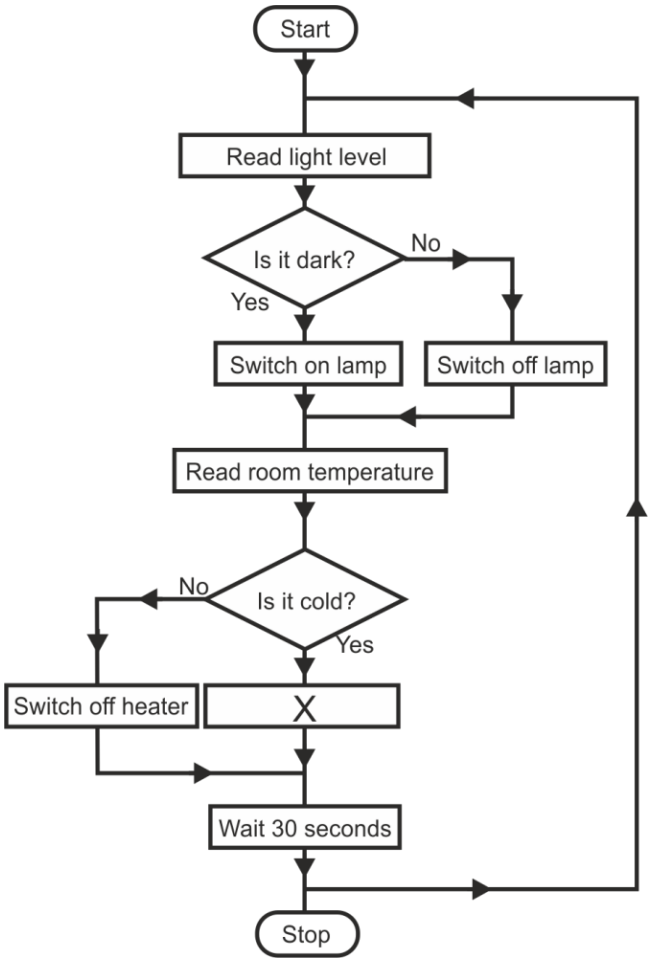
10. A student designs a microcontroller control system to control the heating, lighting and security in a flat. The flowchart for part of the control system is shown below.



(a) (i) State the instruction needed in the box labelled X. [1]

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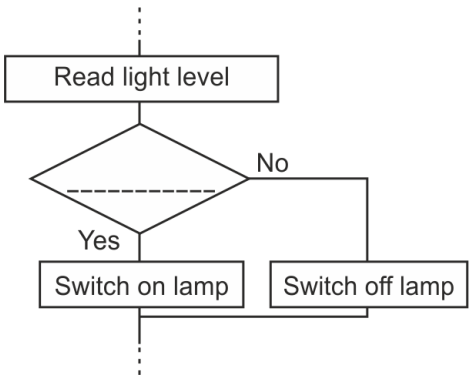
(ii) The system should switch on a reading lamp automatically when it gets dark. The reading from the light sensor is stored in a variable called 'light'. The reading lamp should turn on when 'light' drops to a value below 100_{10}.

Using the template below, rewrite the instruction in the upper decision box in terms of the variable 'light'. [1]



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(b) The microcontroller has two eight-bit ports each of which is bi-directional (can be programed as either an input port or an output port).

(i) Complete the following instructions to turn on the heater. It is connected to bit 7 of Port A and is active-high. [2]

Operator	**Operand**
movlw	b'.....'
.....	.....

(ii) Complete the following section of code so that the three least-significant bits of Port A are configured as inputs and the remaining bits as outputs. [2]

```
bsf     STATUS,RP0
movlw   ……...
movwf   ……...
bcf     STATUS,RP0
```

(c) The system also warns that an intruder has entered the room. The intruder alert is triggered by a 'normally-open' pressure switch in the doorway. When someone stands on the pressure switch, it causes an interrupt.

(i) State why it is better to use an interrupt here, rather than to incorporate this part of the program into the main flowchart. [2]

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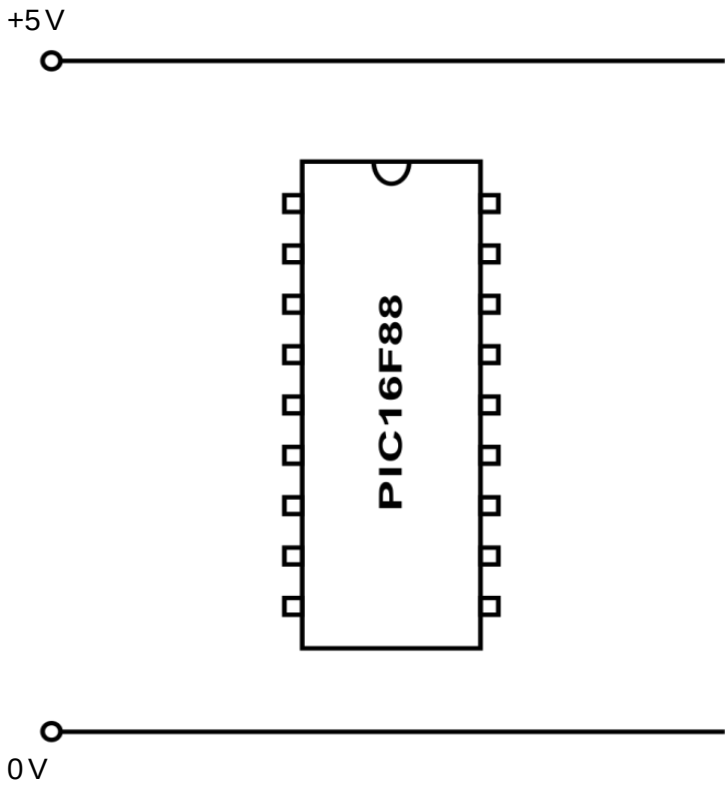
(ii) The microcontroller is configured so that a falling edge signal on RB0 triggers an interrupt. Complete the circuit diagram to show: [4]

- power supply connections to the microcontroller;
- the pressure switch and any other component, connected to the microcontroller, so that an interrupt is caused when someone stands on the pressure switch.



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(d) The interrupt service routine is given below.

- A hidden reset switch is connected to bit 0 of Port A. It is active-high.
- The reading lamp is connected to Port A bit 6.
- The ISR uses a subroutine called ‘onesec’ to cause a one second delay.

Address	**Label**	**Operator**	**Operand**
99	warn	**movwf**	**Wstore**
100	loop	movlw	b’01000000’
101		movwf	PORTA
102		call	onesec
103		clrf	PORTA
104		call	onesec
105		btfss	PORTA,0
106		goto	loop
107		**movf**	**Wstore,0**
108		bcf	INTCON,1
109		retfie	

(i) What is the purpose of the instructions at lines 99 and 107? [2]

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(ii) Evaluate the interrupt service routine for when an intruder enters the room against the details given in (c) and write a specification for any extra features not mentioned. [4]

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11. *(a)* Describe why thyristors, are used to switch high power loads rather than relays. [2]

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(b) A thyristor, suspected of being faulty, is tested using a multimeter connected to a suitable resistance range.

The following procedure takes place.

A. The positive lead from the ohmeter is connected to the anode of the thyristor, and the negative lead to the cathode. The meter reading is noted.

B. With these leads still in position, the gate is momentarily connected to the anode. The meter reading is again noted.

Describe how this procedure can indicate whether or not the thyristor is faulty. [2]

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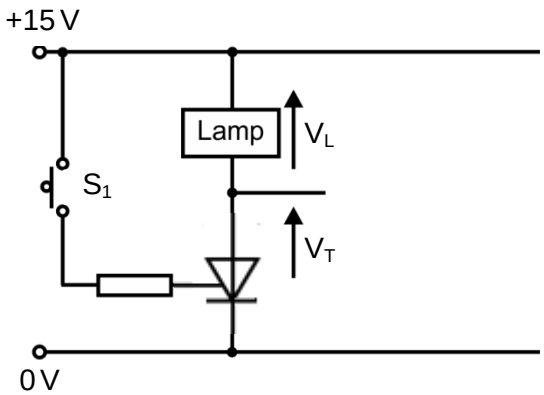
(c) The diagram shows part of a DC circuit in which a thyristor is used to control a lamp.



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(i) Complete the table by adding the values of V_L and V_T when switch S_1 is closed and immediately re-opened. The thyristor is initially switched off. [3]

S_1	**V_T /V**	**V_L /V**
Initially off		
Momentarily on		
Switched off		

(ii) **Complete the circuit diagram** so that the thyristor can be turned off using capacitor commutation. [3]

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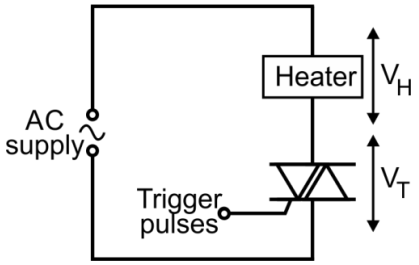
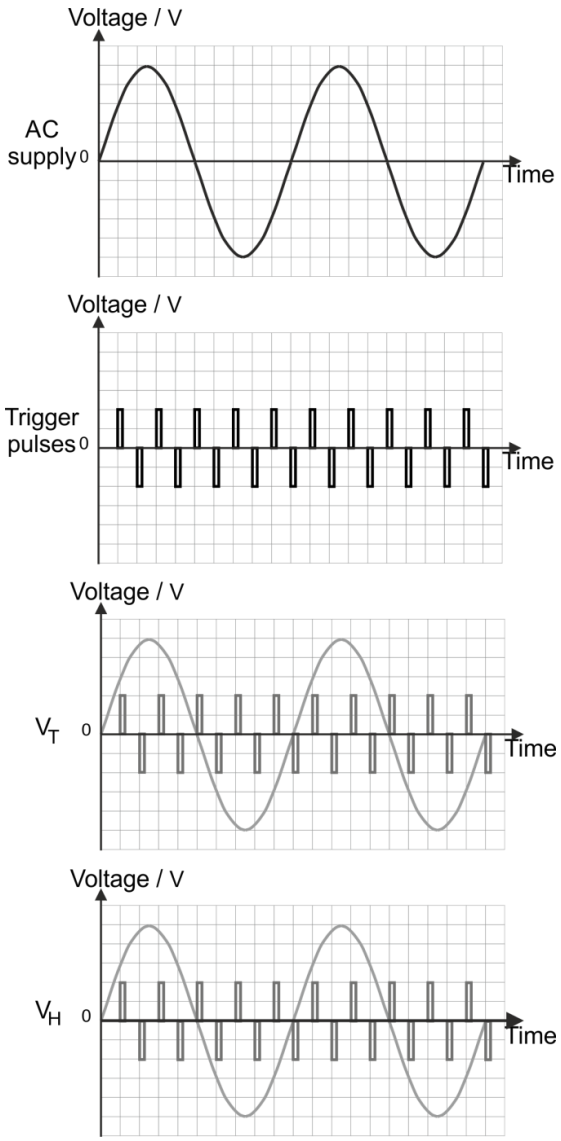
12. The heating element in an electric furnace is controlled by the following triac circuit .



The top graph shows the AC supply voltage.
The second graph shows the trigger pulses applied to the gate of the triac.



Use the axes provided to sketch the resulting waveforms:

(a) V_T, across the triac; [2]
(b) V_H across the heating element. [2]

The graphs include outlines of the AC supply and the trigger pulses to help you.

END OF PAPER

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A LEVEL ELECTRONICS

COMPONENT 2 – Application of Electronics – SAMPLE ASSESSMENT MATERIAL

MARK SCHEME

GENERAL INSTRUCTIONS

Recording of marks

Examiners must mark in red ink.

One tick must equate to one mark (except for the extended response question).

Question totals should be written in the box at the end of the question.

Question totals should be entered onto the grid on the front cover and these should be added to give the script total for each candidate.

Marking rules

All work should be seen to have been marked.

Marking schemes will indicate when explicit working is deemed to be a necessary part of a correct answer.

Crossed out responses not replaced should be marked.

Credit will be given for correct and relevant alternative responses which are not recorded in the mark scheme.

Extended response question

A level of response mark scheme is used. Before applying the mark scheme please read through the whole answer from start to finish. Firstly, decide which level descriptor matches best with the candidate's response: remember that you should be considering the overall quality of the response. Then decide which mark to award within the level. Award the higher mark in the level if there is a good match with both the content statements and the communication statement.

Marking abbreviations

The following may be used in marking schemes or in the marking of scripts to indicate reasons for the marks awarded.

cao = correct answer only
ecf = error carried forward

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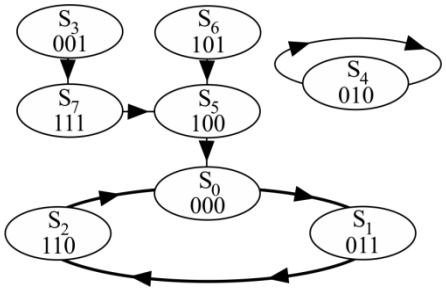
<table>
<tr><th colspan="2" rowspan="2">Question</th><th rowspan="2">Marking details</th><th colspan="4">Marks available</th><th></th></tr>
<tr><th>AO1</th><th>AO2</th><th>AO3</th><th>Total</th><th>Maths</th></tr>
<tr><td>1</td><td>a</td><td>$D_A = C$ (1)
$D_B = \overline{A}$ (1)
$D_C = \overline{B} . \overline{A}$ (1)</td><td></td><td>3</td><td></td><td>3</td><td>3</td></tr>
<tr><td></td><td>b</td><td>
<table>
<tr><th>State</th><th>A</th><th>B</th><th>C</th><th>D_A</th><th>D_B</th><th>D_C</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>1</td><td>1</td><td>1</td><td>0</td></tr>
<tr><td>2</td><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td></tr>
</table>
State 110 (1)
State 011 (1)
</td><td></td><td>2</td><td></td><td>2</td><td>2</td></tr>
<tr><td></td><td>c</td><td>
<table>
<tr><th></th><th colspan="3">Current Outputs</th><th colspan="3">Next Outputs</th></tr>
<tr><th>State</th><th>A</th><th>B</th><th>C</th><th>A</th><th>B</th><th>C</th></tr>
<tr><td>3</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>1</td></tr>
<tr><td>4</td><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td>0</td></tr>
<tr><td>5</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>6</td><td>1</td><td>0</td><td>1</td><td>1</td><td>0</td><td>0</td></tr>
<tr><td>7</td><td>1</td><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td></tr>
</table>
All 5 states correct - 3 marks
Any 4 states correct - 2 marks
Any 3 states correct - 1 mark
1 or 2 states correct – 0 marks
</td><td></td><td>3</td><td></td><td>3</td><td>2</td></tr>
<tr><td></td><td>d</td><td> 

main sequence (1)
unused states (1)</td><td></td><td>2</td><td></td><td>2</td><td></td></tr>
<tr><td></td><td>e</td><td>Defect - stuck state - S_4 (1)
Problem - on start up (1)
Redesigned system - main sequence must be the same (1)</td><td></td><td>1
1</td><td>1</td><td>3</td><td></td></tr>
<tr><td></td><td></td><td>Question 1 total</td><td>0</td><td>12</td><td>1</td><td>13</td><td>7</td></tr>
</table>

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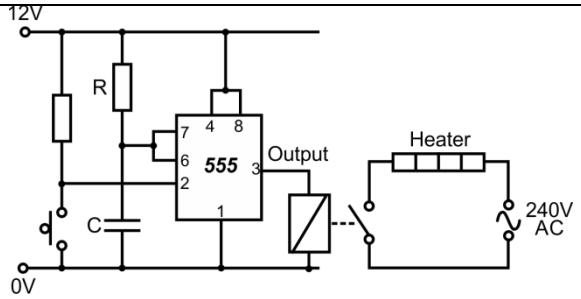
Question			Marking details	Marks available				
				AO1	**AO2**	**AO3**	**Total**	**Maths**
2	*a*		For 10 seconds, buzzer pulses and then stops. (1) While sounding, buzzer is on for 1 s then off for 1 s. (1)		2		2	
	b		 Voltage divider with switch and resistor (1) Correct orientation (1) Relay coil connected correctly (1) Switch added to AC circuit (1)	4			4	
			Question 2 total	**4**	**2**	**0**	**6**	**0**

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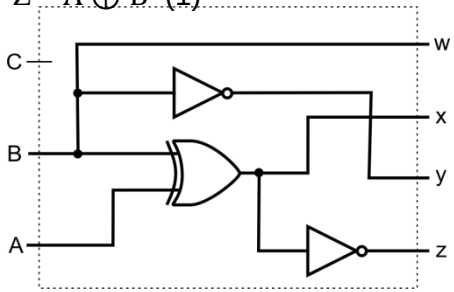
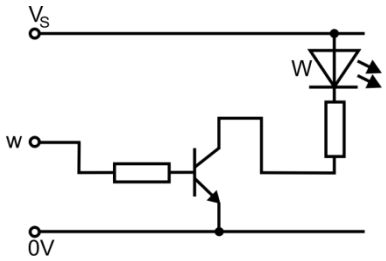
Question			Marking details	Marks available				
				AO1	AO2	AO3	Total	Maths
3	*a*		Output C (1) connected to NOT gate with its output connected to R. (1)		2		2	
	b	i	$W = B$ (1) $X = A \oplus B$ (1) $Y = \overline{B}$ (1) $Z = \overline{A \oplus B}$ (1)  Alternatives: • Use of EX-NOR for z; • Use of NAND gates; • Use of EX-NOR followed by NOT for x. • w connected to B directly 1 mark per correct output ×4	1 1 1 1		4	8	4
	c		 Use of base resistor (1) Correct transistor connections (1)	2			2	
			Question 3 total	**6**	**2**	**4**	**12**	**4**

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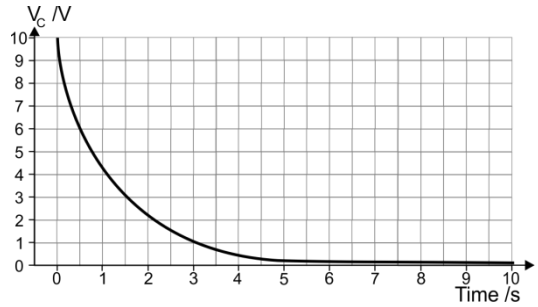
Question			Marking details	Marks available				
				AO1	AO2	AO3	Total	Maths
4	*a*	i	Use of Time constant = $RC = 22\times10^{3}\times47\times10^{-9}$ = 1.03 [s] (1) (or evidence of use of it or of use of full discharge formula) Half-life = 0.69 × time constant = 0.72 s (accept 0.7s) [**ecf**] (1)		2		2	2
		ii	Substitution $t = -RC\ln\left(\frac{V_C}{V_0}\right) = -103\ln\left(\frac{8}{10}\right)$ (1) Correct answer t = 0.23 [s] (accept 0.2) (1)	1	1		2	2
		iii	 Curve of best fit (1) V_C = 10 V at t = 0 s and V_C ~ 0 V at t = 5 s (1) appropriate scales and axes labelled (1)		3		3	3
	b	i	Substitution $\frac{T_{ON}}{T_{OFF}} = \frac{R_1 + R_2}{R_2} = \frac{1+22}{22}$ [1] Correct answer = 1.05 (Accept 1) [1]		2		2	2
		ii	Substitution $t_L = 0.7R_2C = 0.7\times22\times10^{3}\times47\times10^{-6}$ (1) 0.72 [s] (Accept 0.7s) (1)	1	1		2	2
			Question 4 total	**2**	**9**	**0**	**11**	**11**

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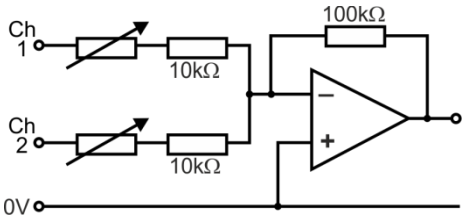
Question			Marking details	Marks available				
				AO1	AO2	AO3	Total	Maths
5	*a*		Bandwidth $= \frac{\text{GBWP}}{\text{Max } g_M} = \frac{1\times10^6}{40}$ = 25 [kHz] (1) Use equal voltage gains for both amp A and amp B Optimum gain = $(400)^{1/2}$ = 20 (1)	1	1		2	1
	b		2 input channels (1) Use of Inv. amp. (1) Correct ratio of resistor values for max. gain (1) Correct value of input resistors to provide correct input impedance (1) Correct circuit diagram (1)  		1	1 1 1 1	5	2
	c	i	Bass boost filter (1) Selection of 300 Ω resistor in formula (1) Substitute into $f_b = \frac{1}{2\pi R C} = \frac{1}{2\pi\, 300\times10^3\; 2.2\times10^{-9}}$ (1) Correct answer = 241 [Hz] (Accept 240Hz) (1)	1 1	1 1		4	2
		ii	Substitute into $G = -\frac{R_F}{R_{IN}} = -\frac{300}{10}$ (1) Correct answer = – 30 (1)	1	1		2	2

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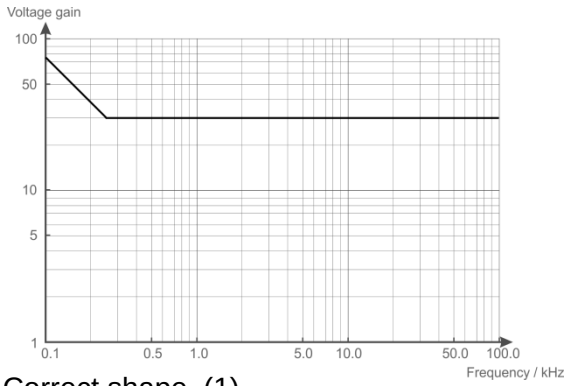
Question			Marking details	Marks available				
				AO1	AO2	AO3	Total	Maths
		iii	 Correct shape (1) Correct break freq. (1) Correct high freq. gain (1)		3		3	2
		iv	Replace 300 kΩ resistor with a variable resistor **or** replace 2.2 nF capacitor with variable capacitor.	1			1	
			Question 5 total	**5**	**8**	**4**	**17**	**9**

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Question			Marking details	Marks available				
				AO1	AO2	AO3	Total	Maths
6	*a*		Any 2 × (1) from: • Greater power output • Higher efficiency • Higher data transmission rate	2			2	
	b		Overall gain = (30 + 20) - (15 x 2) = + 20 dB (1) Manipulation of $G_{dB} = 10\log_{10}\frac{P_{OUT}}{P_{IN}}$ (1) Substitute into $P_{OUT} = 10^{\left(\frac{G}{10}\right)} \times P_{IN} = 10^{\left(\frac{20}{10}\right)} \times 0.2$ (1) Correct answer = 20 [mW] (1)	1	1 1 1		4	4
	c	i	Providing output is not saturated, difference between input voltages ~ V_S / open-loop gain ~ 0 V (1) Non-inverting input is at 0 V so P is at ~0 V.(1)	1	1		2	
		ii	Input impedance of op-amp ~ infinite. (1) No current flows into input so current through photodiode = feedback current (1)	1	1		2	
		iii	Current through feedback resistor = 0.25 mA Voltage across feedback resistor = 0.25 × 10 = 2.5 V so V_{OUT} = +2.5 [V] (1)		1		1	1

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Question			Marking details	Marks available				
				AO1	AO2	AO3	Total	Maths
	d		**Indicative content:** **AO3 allocation (installation and transmitter) –** **The installation** involves short cable runs of ~ hundred metres. The data will consist of emails, images and documents rather than streaming video and so the bandwidth need not be huge. **Transmitter** - Monomode uses laser diodes whereas multimode uses LEDs - much cheaper but slower and wider bandwidth which can cause issues with chromic dispersion. **AO1 allocation –** Fibre - Monomode uses purer glass to reduce attenuation but is more expensive as a result. It does not suffer from modal dispersion, which limits bit rate in multimode fibre. Regenerators - The short cable runs make these unnecessary. Environmental - Monomode fibres are much finer and as a result are susceptible to problems with dust in connectors, which can block the aperture completely. **AO3 allocation (verdict) –** Providing data transmission rates can be kept relatively low, multimode fibres offer a lower cost solution. **5-6 marks** A detailed analysis is given of the factors involved in the installation, including cable length and likely bandwidth requirements. The properties of both fibres and their peripherals are compared in detail. There is a reasoned verdict. *There is a sustained line of reasoning which is coherent, substantiated and logically structured. The information included in the response is relevant to the argument.*	2		2 2		

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Question			Marking details	Marks available				
				AO1	AO2	AO3	Total	Maths
			3-4 marks A general account is given of the factors involved and the relative merits of the two types of fibre. Some attempt is made to justify a decision between the two. *There is a line of reasoning which is partially coherent, supported by some evidence and with some structure. Mainly relevant information is included in the response but there may be some minor errors or the inclusion of some information not relevant to the argument.* **1-2 marks** Little consideration is given to requirements of the installation. The focus is on a comparison of factors involved in the two types of installation. The verdict is unsupported. *There is a basic line of reasoning which is not coherent, supported by limited evidence and with very little structure. There may be significant errors or the inclusion of information not relevant to the argument.* **0 marks** No attempt made or no response worthy of credit.				6	
			Question 6 total	**7**	**6**	**4**	**17**	**5**

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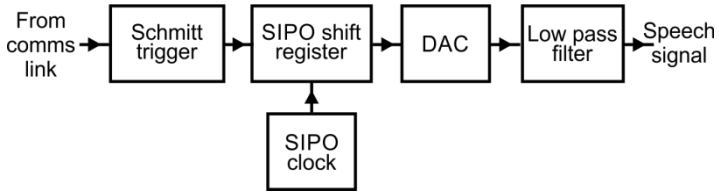
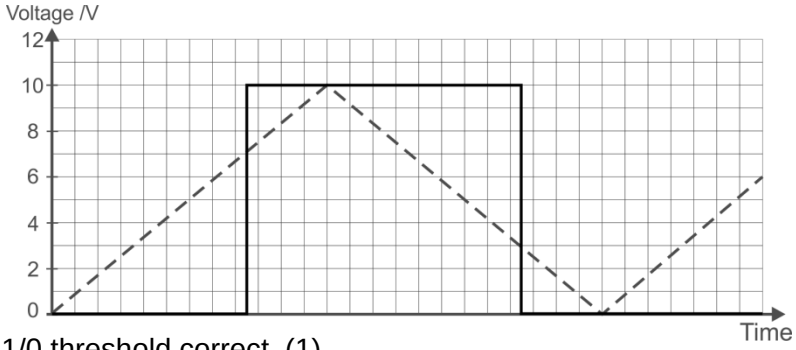
Question			Marking details	Marks available				
				AO1	AO2	AO3	Total	Maths
7	*a*		Sampling clock provides 8000 samples per second. Each sample = 10 bits. PISO shift register has to output 80 000 bits per second. (1) Minimum frequency = 80 kHz (1)		2		2	
	b		 All five blocks correct (3 marks) Four blocks correct (2 marks) Three blocks correct (1 mark) 1 or 2 correct (0 marks)	3			3	
	c	i	 1/0 threshold correct (1) 0/1 threshold correct (1)		2		2	2

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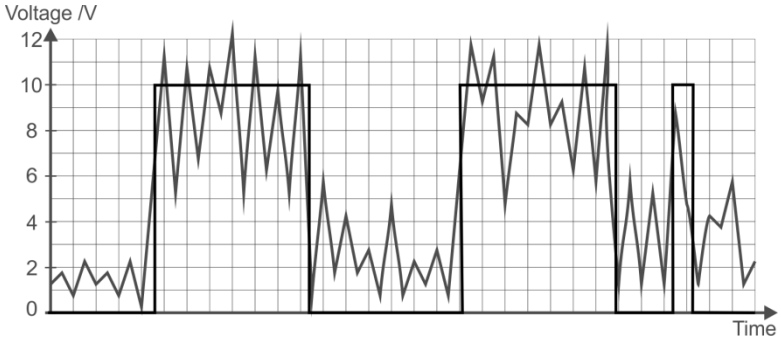
Question			Marking details	Marks available				
				AO1	AO2	AO3	Total	Maths
		ii	 1/0 threshold correct (1) 0/1 threshold correct (1) Correct logic (1) Comment on spurious pulse (1)		4		4	2
			Question 7 total	**3**	**8**	**0**	**11**	**4**

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<table>
<tr><th colspan="3" rowspan="2">Question</th><th rowspan="2">Marking details</th><th colspan="4">Marks available</th><th></th></tr>
<tr><th>AO1</th><th>AO2</th><th>AO3</th><th>Total</th><th>Maths</th></tr>
<tr><td>8</td><td>a</td><td></td><td>Line regulation - output voltage immune to changes in line voltage (1)
Load regulation - output voltage immune to changes in output current (1)</td><td>2</td><td></td><td></td><td>2</td><td></td></tr>
<tr><td></td><td>b</td><td></td><td><table><tr><td>Switches closed</td><td>Total resistance / Ω</td></tr><tr><td>A</td><td>360</td></tr><tr><td>A and B</td><td>180</td></tr><tr><td>A and B and C</td><td>94.7 (accept 95)</td></tr></table>All three correct (2 marks)
two correct (1 mark)
one correct (0 marks)</td><td></td><td>2</td><td></td><td>2</td><td>1</td></tr>
<tr><td></td><td>c</td><td>i</td><td>Substitute into $I = \frac{V}{R} = \frac{12}{181}$ = 66.3 mA (or implied use) (1)
Output voltage $V = IR = 0.0663 \times 180 = 11.9\,[V]$ (1)</td><td>1</td><td>1</td><td></td><td>2</td><td>2</td></tr>
<tr><td></td><td></td><td>ii</td><td>Substitute into $I = \frac{V}{R} = \frac{12}{95.7}$ = = 125.4 mA (or implied use) (1)
Output voltage $V = IR = 0.1254 \times 94.7 = 11.9\,[V]$ (1)</td><td>1</td><td>1</td><td></td><td>2</td><td>2</td></tr>
<tr><td></td><td></td><td></td><td>Question 8 total</td><td>4</td><td>4</td><td>0</td><td>8</td><td>5</td></tr>
</table>

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Question			Marking details	Marks available				
				AO1	AO2	AO3	Total	Maths
9	*a*		V_1 = 12 - 6 = 6 V (1) Substitute into $R = \frac{V}{I} = \frac{6}{0.01}$ (1)] Correct answer = 600 [Ω] (1)	1	1 1		3	2
	b		Substitute into $P = VI = 6 \times 0.01$ (1) Correct answer = 60 [mW] (1)	1	1		2	2
	c	i	When variable resistor =0 Ω V_{OUT} = 6V When variable resistor =15 kΩ $V_{OUT} = 6 \times \frac{(75+15)}{75}$ = 6V (1) Voltage range = 6.0 [V] (1) to 7.2 [V] (1)]		3		3	3
	d		V_{OUT} = 6.0V so resistor chain passes current of $\frac{6}{75}$ = 80 [mA] (1) Total emitter current = 120 + 80 = 200 [mA] (1) Current delivered by op-amp $= I_B = \frac{200}{h_{FE}} = \frac{200}{40}$ = 5 [mA] (1)	1	1 1		3	2
	e		Voltage across zener remains unchanged / additional voltage dropped across R. (1) Output voltage determined by V_Z and so is unchanged. (1)	1	1		2	
			Question 9 total	**4**	**9**	**0**	**13**	**9**

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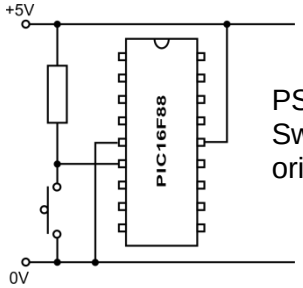
Question			Marking details	Marks available				
				AO1	**AO2**	**AO3**	**Total**	**Maths**
10	*a*	i	Switch on heater		1			
		ii	light < 100		1		2	
	b	i	movlw b'10000000' (1) movwf PORTA (1)	1	1		2	
		ii	bsf STATUS,RP0 movlw b'00000111' (1) movwf TRISA (1) bcf STATUS,RP0	1	1		2	
	c	i	Main program - sensor checked every 30 s. (1) Interrupt - system responds immediately. (1)		2		2	
		ii	 PSU connections x 2 (2) Switch unit (1) oriented correctly (1)	4			4	
	d	i	Protects working register (1) against changes made to it during ISR (1)	2			2	
		ii	Lamp flashes (1) on 1s then off 1s (1) This repeats (1) until the reset switch is pressed. (1)			4	4	
			Question 10 total	**8**	**6**	**4**	**18**	**0**

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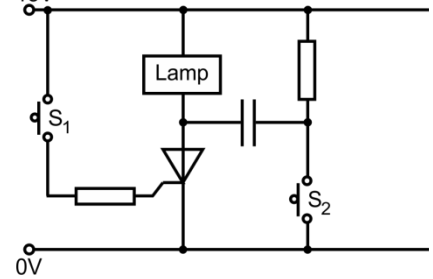
<table>
<tr><th colspan="3" rowspan="2">Question</th><th rowspan="2">Marking details</th><th colspan="4">Marks available</th><th></th></tr>
<tr><th>AO1</th><th>AO2</th><th>AO3</th><th>Total</th><th>Maths</th></tr>
<tr><td>11</td><td>a</td><td></td><td>Thyristors:
are faster switching; (1)
have no moving parts. (1)</td><td>2</td><td></td><td></td><td>2</td><td></td></tr>
<tr><td></td><td>b</td><td></td><td>If working:
• Step A forward biases the thyristor but thyristor does not conduct - high resistance reading. (1)
• Step B sends in gate current to turn thyristor on - low resistance reading. (1)</td><td></td><td>2</td><td></td><td>2</td><td></td></tr>
<tr><td></td><td>c</td><td>i</td><td>
<table>
<tr><th>S_1</th><th>V_T</th><th>V_L</th></tr>
<tr><td>Initially off</td><td>15</td><td>0</td></tr>
<tr><td>Momentarily on</td><td>0</td><td>15</td></tr>
<tr><td>Switched off</td><td>0</td><td>15</td></tr>
</table>
(1)
(1)
(1)</td><td>3</td><td></td><td></td><td>3</td><td></td></tr>
<tr><td></td><td></td><td>ii</td><td>+15V
 

Second switch unit added (1)
Correct orientation (1)
Capacitor added in correct position (1)</td><td>3</td><td></td><td></td><td>3</td><td></td></tr>
<tr><td></td><td></td><td></td><td>Question 11 total</td><td>8</td><td>2</td><td>0</td><td>10</td><td>0</td></tr>
</table>

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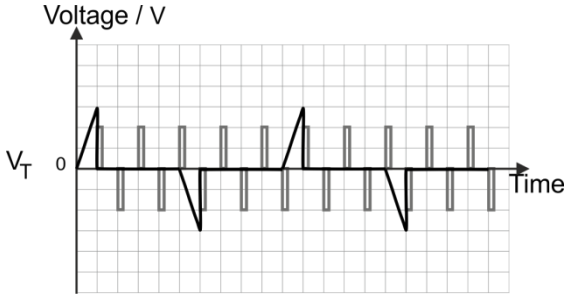
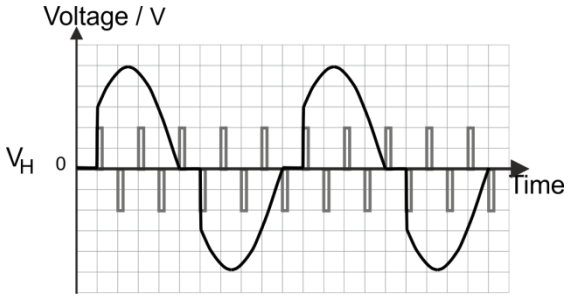
Question			Marking details	Marks available				
				AO1	AO2	AO3	Total	Maths
12	*a*		 Correct shape (1) Correct synchronisation (1)	2			2	1
	b		 Correct shape (1) Correct synchronisation (1)		2		2	1
			Question 12 total	**2**	**2**	**0**	**4**	**2**
			TOTAL	**53**	**70**	**17**	**140**	**56**

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