GCSE EXAMINERS' REPORTS

ELECTRONICS
GCSE

SUMMER 2022

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ELECTRONICS

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COMPONENT 1: PRINCIPLES OF ELECTRONICS

General Comments

The number of candidates sitting the paper compared to the last examination in 2019 has decreased slightly.

A full range of marks from 1 to 80 was observed. The facility factor shows similar accessibility to previous years. Statistical data showed that question 1 was the most accessible (FF 75.6) with question 5 being least accessible (FF 49.2).

Comments on individual questions/sections

Q.1 **(a)** Most candidates scored well on this question. Apart from using the wrong symbol, other errors were only one input line and failing to add an output line.

(b) **(i)** Surprisingly, a number of candidates made errors completing the truth table for X and Y despite these just being the inverse of A and B respectively. This error made Q much more difficult although error carried forward (ecf) was applied where appropriate.

(ii) This question proved difficult for many candidates who had made mistakes in (b) (i). There were a number of answers that had little resemblance to the output Q.

(c) There were a good number of correct answers given to this question.

(d) Again, another well answered question.

Q.2 **(a)** Usually a well answered question but a number of candidates found this question difficult. A significant number had no issues and scored full marks.

(b) This was very well answered by many candidates, but some candidates were unable to produce the NAND equivalent of a NOT gate. Being unable to correctly convert the circuit to NAND gates made it very difficult to identify redundant gates but where possible ecf was applied.

(c) Only a minority of candidates were able to justify the reason for reducing logic circuits to NAND gates, and these were usually the higher scoring candidates overall.

Q.3 Overall this question was either answered very well or very poorly, highlighting some possible gaps in candidates' knowledge.

(a) This was answered well by most candidates, the common error was to use orange as the Band 3 colour instead of red.

(b) This was generally either all correct or mostly incorrect. The most common error was to neglect the multiplier.

(c) This question was normally correct or omitted all together.

Q.4 **(a)** The majority of candidates scored full marks on this part of the question. Common errors were thinking that the Latch was an output device, and the solenoid was an input device.

(b) The QER question was answered very well by many candidates, but some showed a lack of knowledge of how to “evaluate”. This produced answers that lacked structure and the ability to explain how the block diagram functioned in relation to the design specification. This resulted in many low band answers. More able candidates provided high quality answers and had clearly understood the command “evaluate”. These candidates scored highly on this part of the question.

Q.5 This question focused on a potential divider and a Zener circuit.

(a) The common mistakes with this question were to use the 6.2kΩ instead of 6.8kΩ on the top of the voltage divider formula, or to neglect multiplying by the input voltage.

(b) This part was poorly answered and indicated that they did not recognise the symbol or function of the zener diode, as many candidates gave the answer as 9V - (a) and scored zero marks.

(c) Omitted by a significant number of candidates. Some of those that did attempt it were unable/unaware of the method to determine the resistance of the parallel combination of 6.8kΩ and 1kΩ using the answer in the voltage divider formula to determine the new $V_{OUT(A)}$. As with part (b) not recognising the function of a zener diode led to many candidates attempting an incorrect method to determine $V_{OUT(B)}$.

(d) This part resulted in a range of answers, which reflected success from parts (b) and (c).

Q.6 Those that attempted the question rarely scored full marks although some achieved full marks.

(a) In this part, it was disappointing to see the number of candidates unable to read the resistance of the LDR from the graph. Some of the lines drawn on the graph from 60 lux and the intercept with the characteristic line were not near to vertical or horizontal demonstrating poor understanding of graph reading skills.

(b) It was rare to see the voltage divider formula, or used with the correct resistor values by candidates.

(c) Candidates often gave answers too far away from the switching point to gain full marks.

(d) The choice of the correct formula proved too challenging for many, over complicating calculations by using $P=V^2/R$, rather than the more straightforward P=IV. Some used the method successfully and scored full marks. Others stumbled halfway and only achieved partial success.

(e) Some candidates were only able to write down the correct formula, failing to substitute the correct values therefore scoring few marks. For the candidates that knew what they were doing this resulted in 4 straightforward marks.

Q.7 In this basic transistor switch circuit question many candidates struggled to recall the necessary basic theory.

(a) Few candidates used the fact that the transistor was saturated, therefore V_{CE} was 0V making the voltage across the motor to be 12V, the use of 0.7 was very common here.

(b) **(i)** Candidates often ignored the $IC=H_{FE} \times I_B$ formula, somehow bringing in power formulae and scoring zero marks.

(ii) There were limited correct answers, ecf was applied from (b)(i) where possible.

(c) Candidates demonstrated a lack of understanding of the transistor switch and remembering that V_{BE} is 0.7V.

(d) Candidates needed to add the answers to (b) & (c) together, but again this was rare in all but the strongest candidates.

Summary of key points

- Candidates need to read the question carefully as some questions require work on part completed diagrams or graphs, instead of written answers directly under the question.
- Candidates need to learn equations that are not provided on the information sheet, e.g. V=IR, P=VI, $P=I^2R$ etc.
- Candidates need to be given opportunities to draw standard circuits from memory – e.g. NAND equivalent circuits of all standard AND, OR & NOT gates.
- Candidates should be shown how to read graphs, and how to draw vertical and horizontal lines to reach the correct points and an axis, and to look at the label to select the correct units.
- Candidates should check if an answer is likely, e.g. the voltage across a resistor is unlikely to be 9900V, when the power supply is 12V.
- Candidates need to understand that units should be provided in their answers.

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COMPONENT 2: APPLICATION OF ELECTRONICS

General Comments

The paper has performed well, producing a range of marks from 1 to 80. The facility factor shows similar accessibility to 2019. Statistical data showed that Question 1 was the most accessible (FF 78.8) with Question 7 being least accessible (FF 41.3).

Comments on individual questions/sections

Q.1 (a) This proved to be a very successful question for the vast majority of candidates.

(b) A number of candidates joined the “No” branches back to the command boxes rather than the main program, indicating for example that the already open water valve should be opened again and therefore lost a mark.

Q.2 (a) Some different solutions were presented many of which were hybrids of monostable and astable 555 designs. Marks were assigned for the use of a push to break switch, orientation of trigger and connection to pin 2, then separately for the timing circuit and connection to pin 6 and 7. Most candidates scored some marks on this question but only the highest achieving candidates were able to achieve full marks.

(b) (i) This part was poorly attempted with many not able to select the correct formula and scored zero marks. Those that did choose the correct formula then had issues with the multipliers, again getting an incorrect answer but gaining some processing marks.

(ii) This part was marked independently so provided the answer was the closest to the answer given in part (i) a mark was awarded.

(c) (i) Well answered by the majority of candidates, the most common error was to miss out the number 0 from the 430.

(ii) Poorly answered with many candidates being unable to recall $P=I^2R$, and unable to use the ‘m’ multiplier resulted in many candidates scoring low marks on this question.

Q.3 (a) There were two major difficulties for candidates on this part of the question, firstly correctly identifying it as an inverting amplifier in order to select the correct formula, and secondly realising that minimum gain is when the variable resistor is set to zero, many thought the minimum was 1k. Similarly, selecting the maximum gain is when the variable is a maximum of 100k.

(b) Candidates' ability to draw a sinusoidal signal have not improved but their answers were marked independently for correct amplitude, signal inversion and signal frequency within 1 small square of the actual result. Candidates achieved a range of marks on this question.

(c) Some candidates achieved full marks but many were unable to select the correct formula, saturation voltage, or max gain.

Q.4 **(a)** This question was well attempted by the majority of candidates who scored 4 marks. The biggest issue was candidates forgot about the reset and the cycle repeating and lost a mark.

(b) This question was all about resetting a counter on a specific number and had four discrete marking points. The most common error was missing the invert 'o' symbol on the reset pin and therefore choosing an AND gate over the required NAND. The majority of candidates scored some marks on this part of the question.

Q.5 This question was related to D-types and astables, the question carried a considerable number of marks.

(a) A number of candidates only produced a counter output for the output instead of the data transfer that was required and some lost marks for too many transitions. Most scored 1 mark for starting at logic 0.

(b) **(i)** There was a wide variation in the quality of the circuit diagrams completed, very few marks were awarded between 1 and 4. Candidates need to understand how to complete these basic circuits.

(ii) A significant number of candidates did not take up the option of a straightforward mark of labelling the rising edge of the pulse generator output and omitted this completely. For Q_A those that attempted the question completed this correctly and gained 3 marks. For Q_B those that attempted this part had the transition points and had them on the rising edges of Q_A instead of the falling edges and lost two marks. Other candidates provided the inverse of Q_A and scored 0.

(c) Candidates' poor graph reading skills and not knowing the difference between the mark and space led to many incorrect answers. Part (c)(iii) was well answered by many candidates but provided a challenge for a significant number where this application of the determination of resistor values for a 555 timer clearly was misunderstood.

Q.6 **(a)** As with the 2-bit counter diagram covered earlier, the number of correct non-inverting amplifiers was primarily reserved to the candidates working at the top end of the mark range. Those that attempted a diagram may have gained a mark for a correct R_F.

(b) In a similar fashion some candidates used the wrong formula, whilst others had the right formula and ratio but neglected to give values that were over 1kΩ.

(c) Generally, candidates scored one of the 3 marks for having the maximum gain, but many neglected to calculate the 70% gain at 25kHz in order to provide the critical point of transfer in the gain falloff from the maximum.

Q.7 As with component 1 the response by many candidates showed a misunderstanding of the word “evaluate”. For others, the question caused no issues and extremely well written evaluations were observed scoring full marks.

Summary of key points

- Candidates need greater understanding of the role of links in flow charts to ensure that they feedback to an appropriate part of the program and that this is not always the start.
- Candidates need to understand that they will be required to draw standard circuits for basic counters, 555 monostables and astables, inverting, non-inverting and summing amplifiers.
- Candidates need to practice the use multipliers such as kΩ, and μF in equations.
- Candidates need to practice rearranging equations that contain bracketed terms, in particular $I_D = g_M (V_{GS} – 3)$.
- Candidates need to practice answering ‘Evaluate’ questions which must start with a detailed comparison between the specification and the design.

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COMPONENT 3: EXTENDED SYSTEM DESIGN AND REALISATION TASK - NEA

General Comments

Centres are to be thanked for their effort in presenting candidates' work for moderation, and for recording the marks online.

The assessment of the work was within tolerance for most centres but in some centres adjustments to marks were required.

The candidates of most centres produced a very good range of projects.

Some centres did not provide any annotation of candidates' work. Annotation on the scripts and/or mark scheme would greatly aid the moderation process. In particular an indication on the mark scheme of which level descriptors were or were not achieved would be very helpful.

Some centres seem to be providing a prescriptive template for reports. This should be avoided where possible as this guidance can limit the mark awarded to the candidate.

Comments on individual questions/sections

System Planning

In several centres all candidates' work seems to have focused on a common theme. Candidates should focus on an individually identified problem to analyse to enable them to write a design specification based on the problem. This is expected to produce a wide range of tasks within a centre.

Design specifications should contain a range of both qualitative and quantitative terms based on their analysis of the problem and contain detailed realistic electronic parameters. Unless very good reasons are provided as justification, neither the battery supply voltage nor the number of components should be considered as quantitative specifications. The choice of a particular component may be part of the design solution to a problem but not part of the specification.

In some centres candidates seem to have put a great deal of effort into providing information that earned very little marks. Examples included extensive research replicating commercially available devices and components that were outside their experience. This research was not used in the projects. Many candidates provided multiple photographs of input and output devices that were not required for their design.

System Development

The block diagram for the proposed system can be modelled using systems boards or a systems simulation package. This will allow candidates to modify their design to achieve their specification.

Once the final system block diagram is finalised the emphasis should then be on building and testing individual sub-systems which can then be interconnected to form the complete system.

Many of the accounts provided for the sub-system testing tended to be observational with limited account of the testing that took place. For each sub-system a test reading should be provided with the output activated and non-activated.

Awarding accurate marks is critical to ensure that candidates receive fair and consistent reward for the work produced. Banded mark descriptors help to determine the correct band where a candidate’s work fits. Some centres awarded top band marks for development when there were less than five different sub-systems developed.

Test results obtained from circuit simulations are only valid if real components such as LM741 or BC548 are chosen rather than the generic IC1 and Q1.

When using a flowchart program, simulation tests should be carried out for the program and include screenshots of the results.

The final circuit should be one complete system where there is signal transfer between each sub-system, rather than between two independent systems.

System Realisation

The adaptations for summer 2022 only, allowed learners to complete their final circuit by using circuit simulation if they were unable to build a complete physical circuit. If physical circuits were not completed, then an organised physical layout for the circuit was required to gain the layout marks. This meant that a planning diagram of the breadboard, stripboard or printed circuit board was required.

To gain the full range of marks for system realisation candidates must have very well organised physical circuit layouts (rather than a circuit diagram) with wires and components arranged vertically/horizontally to a high standard.

As was the case with sub-system testing, the account provided for the complete hard wired system testing tended to be observational with limited use of test equipment. The recording of test results tended to lack detail. Much of the analysis of the results was superficial.

To access the full range of marks for system realisation candidates should use appropriate test equipment, then record and analyse the numerical results.

Evaluation

A consequence of not having any realistic measurable parameters in the specifications resulted in a significant minority of candidates providing very simplistic evaluations. To gain the full range of marks candidates must make valid critical and objective evaluations of performance.

The evaluation should compare the system against the design specification and make suggestions for improvement to access the full range of marks.

Summary of key points

- Annotation on the scripts and/or mark scheme would greatly aid the moderation process.
- Candidates should focus on a problem to analyse to enable them to write a design specification based on an individually identified problem.
- Candidates should be taught how to structure their reports rather than using prescriptive templates. Mini tasks given to candidates during the teaching of the course can be used to build up skills in structuring their reports, such as identifying a problem and preparing a design specification of the problem or producing results of tests and analysis for a set circuit that the candidates have worked on.
- Proportionate time needs to be spent on all aspects of the NEA. Candidates in some centres spent too much time on research and investigation activities, which were not very relevant. The work expended on this was often to the detriment of the testing and development activities. This resulted in limited analysis of the results. Guidance on NEA reports can be found in the 2019 and 2020 CPD available on the Secure Website.

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