GCSE EXAMINERS' REPORTS

ELECTRONICS (LEGACY)

SUMMER 2018

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E1

General comments

The paper performed well producing a spread of marks from 11 to 59 out of the 60 marks available on the paper. Despite no candidate achieving full marks, correct answers were observed to all questions.

Detailed comments

Q1. Most candidates scored well on this question as it was meant to provide a gentle introduction to the paper. In part (a) however a significant number of candidates gave the answer of 'thyristor' instead of 'transistor', and 'led' instead of 'diode' which was quite surprising after two years of study.

In part (b) there were a number of candidates that could not organise the sub-systems provided into their 'input-processing-output' functions which again caused some surprise to the marking team. There was no particular sub-system that was incorrectly placed, the errors appeared random almost as if candidates were guessing rather than using any specific knowledge gained throughout the course.

Q2. This question was answered well and much better than in previous years. Only a small number of pupils made errors, and these were mostly related to the voltages across the components. Only a handful of candidates showed no understanding giving random and unconnected answers.

Q3. Candidates generally scored well on this question either with a perfect score of 3/3 or through the use of ecf gaining 2/3 marks because the PIN numbers were incorrectly identified on the IC. Those who lost marks on parts (b) and (c) ticked either random boxes or ticked those for every input or output rather than for the specific gates required.

Q4. This was a very successful question for candidates with the overwhelming majority scoring full marks.

Q5. The questions tested the candidate's knowledge of the names of the connections for a MOSFET and this revealed that approximately 25% of candidates were unable to select the correctly labelled symbol.

Q6. This proved to be a very successful question for candidates with very few failing to score full marks. On the few occasions when mistakes were made they tended to be in the number of zeros column, but it is difficult to explain why this is the case apart from a lack of care on the part of the candidates when selecting their answer.

Q7. This was a well answered question with the majority of candidates scoring full marks. The use of base units may have contributed to the success here as no standard multipliers were involved in the calculation and it was extremely rare to find an incorrect answer.

Q8. Most candidates apart from the very weak were able to score well on parts (a) and (b). Part (c) however caused many candidates some difficulty as they often gave the incorrect answer that V_Y would decrease. In part (d) similarly candidates found it hard to explain what would cause the voltage V_Y to decrease, i.e a lowering of the light level or increase in resistance of X being acceptable answers, and therefore it would appear that a good number of candidates do not understand the operation of a light sensing circuit.

Q9. This was a very good differentiating question as candidates either scored very well or very poorly. Those who scored well usually had full marks or lost one mark through the inclusion of a thyristor as the output driver instead of the transistor switch. Those who fared less well on the question appeared to be just putting random sub-systems into the block diagram gaining the 'odd' mark purely by chance as the systems being used in parts of their design had no link to the specification whatsoever e.g. delay unit and temperature sensing unit.

Q10. This was also a successful question for the majority with part (a) almost universally being correct with a small minority giving the incorrect answer of 'NOR' for part (b).

Q11. This was answered well by the majority of candidates who scored at least 2/3 marks in part (a). The most difficult part was selecting the gate for providing the output Q from inputs X and Y, with those who did make a mistake on this part selecting an AND gate instead of the required NOR. Part (b) caused few problems with nearly all candidates giving the correct answer.

Q12. The NAND gate reduction exercise has proved in recent years to be a problem for a good number of candidates, but this seems to be causing less of a problem with nearly all candidates now being able to identify the redundant gates. A very small number of candidates now have no idea what they are looking for and tick the majority of gates and scored no marks.

Q13. Use of the rules for determining the effective resistance of resistors in series and parallel is an important skill in electronics and it is very pleasing to see the number of candidates that can now correctly determine the resistance of both series and parallel networks. The number of correct responses to this type of question has been growing over the years and now virtually all candidates are scoring at least 2/3 marks.

Q14. The use of Boolean algebra is a higher level concept but a significant number of pupils scored well on this question with only a minority failing to score any marks at all. There were a few candidates that correctly answered part (a) but then made no attempt at part (b) which was strange, at the very least you would expect candidates to 'guess' as there were only four possible answers and candidates could have just ticked any one for a 25% better chance of gaining a mark instead of failing to attempt it at all.

Q15. This question split the candidates into those who knew the NAND equivalent circuits and those that didn't. Whilst a good number had no issues at all, there were some who clearly had no idea and scored 0.

Q16. Candidates found this question to be quite difficult. Part (a) (i) was completed correctly by the majority of candidates who identified the correct equation, however when putting the equation to use gave an incorrect answer of 4 instead of 4.1 caused by rounding 4.086 down instead of up.

Part (b) proved to be a very good discriminator and very few candidates came close to the correct answers. Too many candidates focussed on cost, or the fact that it was easier to calculate V_{OUT} but I'm not sure why they thought this as the same calculation would need to be done. Only a handful of pupils identified either the fact that V_{OUT} could be altered without changing components and hardly any explained that the full input voltage range was now available for V_{OUT}.

Q17. This question tested candidate's ability to design voltage dividers and sensing circuits. In part (a) candidates had to design a voltage divider to produce a voltage of 3 V. This restricted the choice of resistors to the 3 kΩ and 12 kΩ. Any other resistor combination in this part scored 0. An ecf mark was given for the inversion of the 12 kΩ and 3 kΩ resistors.

In part (b) candidates needed to select the thermistor with any of the fixed resistors with correct orientation scoring full marks and an inverted arrangement scoring 1 ecf mark.

In part (c) candidates were required to explain that one of the fixed resistors needed to be 'changed' or 'replaced' with a variable resistor to allow the temperature at which the output became active could be adjusted. Simply giving an answer of 'use a variable' was insufficient for a mark.

Q18. Part (a) was answered well on the whole and the majority of candidates answered this correctly. In part (b) however, a good number of candidates selected the incorrect equation $\left(\frac{2}{25}\right)$ instead of the correct $\left(\frac{4}{25}\right)$ losing them a mark. This lead to an incorrect answer for (c) again causing the loss of a mark. In part (d) an ecf mark became available for correctly giving the nearest preferred value resistor in ohms that was above the calculated value in kΩ.

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E2

General comments

Overall, a very creditable performance from most candidates with some outstanding results.

The most challenging topics were, as in previous years, some timing diagrams, Schmitt inverters, memory organisation and transistor calculations. Again, performance seems to be centre-dependent. Some need to offer more, structured practice on these topics.

It is disappointing to see candidates offer totally unrealistic answers, such as a voltage drop of 1464 V across a resistor in a circuit powered from a 9 V battery.

Detailed comments

Q1. Part (a) - Some drew two lines from a subsystem to an application. These automatically lost that mark.

Part (b) - Many were tempted by the first option - "…changes instantly and then stays there." to describe the behaviour of a monostable.

Part (c) - Most answers were correct but some candidates chose the first option, perhaps tempted by the inclusion of the switch.

Q2. Part (a) was usually answered correctly but part (b) - a calculation - caused problems for some.

Q3. Answers to parts (a) and (b) were almost universally correct. A tiny minority used 'ticks' to indicate the logic 1 segments and blanks for the logic 0 segments. These answers were not accepted. Part (c) proved more difficult with many attracted by the "Reset" option.

Q4. This was not-well answered, with candidates not wanting to give the same answer - "digital" - for three consecutive answers?

Q5. Part (a) was not well-answered with all distractors tempting to some.

Part (b) - The rows for pulses 1, 2 and 3 were usually correct, though some filled up the cells from the left with "on". The bottom row was often "off", "off", "off", "off".

Q6. The vast majority answered both parts correctly.

Q7. Part (a) - mistakes seemed to be the result of misreading the options.

Part (b) - most timing diagrams were completely correct. Some graphs used falling edges of the clock pulse, even though they had identified the rising edges correctly in the previous question.

Q8. Some annotated their answer with a binary count to help them to answer the questions - a good technique. The timing diagrams in part (a) were usually incorrect, for a range of reasons. More identified the binary count at 'T' correctly.

Q9. Most answers were completely correct. A tiny minority were totally wrong, suggesting unfamiliarity with flowcharts.

Q10. Neither part was well-answered. Many believing the comparator has two switching thresholds.

Q11. Part (a) - Many confused options 'A' and 'E' in part (i) and 'B' and 'E' in parts (ii) and (iii).

Part (b) - Most chose the correct formula but some could not calculate the answer correctly. Some chose option 4, where the input voltages were reversed.

Q12. Part (a) - "36" was a popular distractor, some candidates believing that voltage gain is additive.

Part (b) - Many forgot that the amplifier was inverting and omitted the '– ' sign.

Part (c) - The popular distractor was "6.0" - arithmetic?

Q13. Not well-answered, particularly part (c).

Q14. Parts (a) and (b) were usually correct but part (c) caused problems. In part (d), some chose a NOT gate even though the diagram showed that the gate had **two** inputs.

Q15. The responses were excellent from most candidates but candidates from a few centres struggled with this question. A common error was to assume that 0V represented logic 0. Some ignored the fact that it was a Schmitt **inverter**.

Q16. Some candidates chose to invert the initial signal which again seemed to be centre-dependent. Some answers introduced an unwanted phase shift. In part (b), many chose the inverting amplifier circuit diagram or formula.

Q17. Not well-answered, with only a few scoring full marks. Some gained credit in part (b)(ii) by adding 0.7 V to their incorrect answer to (b)(i).

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E3

General Comments

Thanks are extended to centres for their effort in both organising candidates' work for moderation and the online recording of centre marks.

Candidates produced a very good range of projects. Some of the work was outstanding and demonstrated considerable innovation.

The majority of centres provided both excellent annotation and excellent photographic evidence, which aided the moderation process. A small number of centres still persist in not providing any annotation.

The assessment of the work was within tolerance in the majority of centres with only a very small percentage requiring adjustment of their marks The main cause of adjustment was due centres tending to give candidates the benefit of the doubt on nearly all borderline decisions.

Specific comments

The following points are made to highlight the more commonly misunderstood criteria contained in the Controlled Assessment Mark Booklet:

1. Project brief and specification:

1d/e: Specifications should contain a range of both qualitative and quantitative terms based on their analysis of the problem and contain realistic measurable electronic parameters.

2. Project planning and research:

2a/b: Responses in this section continue to be consistently weak. Searching the internet/ textbooks for general information about standard components/ component costings / truth tables of standard logic gates etc. is not considered relevant research.

3. Project development:

3j/o/s: These are higher order skills designed to challenge the more able candidates. In the vast majority of cases no reference of current or power was mentioned in the specification, hence neither the measurement nor the calculations were relevant. A suitable example could be to measure the current drawn by a solenoid when connected across the power source to find a suitable transducer driver.

3m/n/o: The tests referred to in these sections must be carried out on the final completed breadboard/stripboard/PCB circuit.

4. Performance of the hardwired system:

4g A consequence of not having many measurable parameters in the specifications resulted in a number of candidates producing very simplistic evaluations.

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