GCE A Level Examiners' Report

Electronics

A level

Summer 2025

Introduction

Our Principal examiners' report provides valuable feedback on the recent assessment series. It has been written by our Principal Examiners and Principal Moderators after the completion of marking and moderation, and details how candidates have performed in each component.

This report opens with a summary of candidates' performance, including the assessment objectives/skills/topics/themes being tested, and highlights the characteristics of successful performance and where performance could be improved. It then looks in detail at each unit, pinpointing aspects that proved challenging to some candidates and suggesting some reasons as to why that might be.[1]

The information found in this report provides valuable insight for practitioners to support their teaching and learning activity. We would also encourage practitioners to share this document – in its entirety or in part – with their learners to help with exam preparation, to understand how to avoid pitfalls and to add to their revision toolbox.

Further support

Document	Description	Link
Professional Learning / CPD	Eduqas offers an extensive programme of online and face-to-face Professional Learning events. Access interactive feedback, review example candidate responses, gain practical ideas for the classroom and put questions to our dedicated team by registering for one of our events here.	https://www.eduqas.co.uk/home/professional-learning/
Past papers	Access the bank of past papers for this qualification, including the most recent assessments. Please note that we do not make past papers available on the public website until 12 months after the examination.	Portal by WJEC or on the Eduqas subject page
Grade boundary information	Grade boundaries are the minimum number of marks needed to achieve each grade. For linear specifications, a single grade is awarded for the subject, rather than for each component that contributes towards the overall grade. Grade boundaries are published on results day.	For unitised specifications click here: Results and Grade Boundaries and PRS (eduqas.co.uk)

[1] ***Please note that where overall performance on a question/question part was considered good, with no particular areas to highlight, these questions have not been included in the report.***

Exam Results Analysis	Eduqas provides information to examination centres via the WJEC Portal. This is restricted to centre staff only. Access is granted to centre staff by the Examinations Officer at the centre.	Portal by WJEC
Classroom Resources	Access our extensive range of FREE classroom resources, including blended learning materials, exam walk-throughs and knowledge organisers to support teaching and learning.	https://resources.eduqas.co.uk/
Bank of Professional Learning materials	Access our bank of Professional Learning materials from previous events from our secure website and additional pre-recorded materials available in the public domain.	Portal by WJEC or on the Eduqas subject page.
Become an examiner with WJEC.	We are always looking to recruit new examiners or moderators. These opportunities can provide you with valuable insight into the assessment process, enhance your skill set, increase your understanding of your subject and inform your teaching.	Become an Examiner | Eduqas

Contents

Executive Summary

Candidates' performance in A level Electronics this year was slightly better than last year. The mean marks in all three components were slightly higher than in 2024. Analysis of responses to questions showed the level of difficulty of the Component 1 and 2 exams to be similar to 2024.

Component 1 & 2 exams

Both exams covered all assessment objectives and all topics in the specification, including some synoptic questions. The standard was in line with previous years.

Most candidates' responses showed a high level of knowledge and preparation. Calculations were usually well laid out, showing intermediate steps and correct use of multipliers. Most circuit diagrams were accurately drawn in pencil, although a minority of candidates did not use a ruler.

In Component 1, candidates performed well in the questions on combinational logic, comparators, MOSFETs and inverting amplifiers. In Component 2 the highest marks were achieved in questions on monostable circuits, sequence generators, microprocessors and audio mixers.

In Component 1 lower marks were gained in questions on band-pass filters, slotted discs and communication systems. In Component 2 candidates gained lowest marks in questions on PCM/TDM and the QER question on a voltage regulator. Performance in the QER questions varied widely. There were some very good answers but many were too vague.

The A level Electronics eBook includes examples and exercises on all topics. This is available on the resources section of the AS/A level Electronics webpage.

Component 3 NEA

Most centres' samples were well organised and presented promptly. Candidates' marks were recorded accurately. The marking criteria were generally well understood and applied consistently. Only a small number of centres' marks required adjustment. It was evident that some centres had acted on advice given in previous years' moderator reports.

Candidates must choose their own problem, appropriate for their ability, which should allow them to produce a full design specification. Some candidates provided poor specifications with insufficient qualitative/quantitative parameters. Research should be based on the chosen problem and inform the specification.

Most of centres provided excellent photographic evidence of final circuits and the stages of development and testing. However, some images of circuits were too small or unclear.

As in previous years most marks were lost for the Evaluation section. To access the higher marks, circuits must be tested and evaluated against the specification. A poor evaluation was often the consequence of too few measurable parameters in the specification. Improvements must be relevant and candidates should state how they would be beneficial.

From summer 2026, NEA samples must be uploaded electronically to IAMIS rather than posted to moderators. Clear annotation of mark schemes and candidates' work, showing which criteria have been achieved, will greatly aid the online moderation process.

A LEVEL ELECTRONICS

GCE A level

Summer 2025

Component 1 – Principles of Electronics

Overview of the Component

The examination paper covered all assessment objectives AO1, AO2 and AO3 as well as coverage across the Component 1 specification. The standard was in line with previous years.

Candidates' responses showed a high level of preparation for the examination and a high level of knowledge was evident for the vast majority of candidates. Calculations were usually well laid out and easy to follow. Circuit diagrams were mostly well-drawn and accurate although a minority of candidates still refuse to use a ruler. There was a definite improvement in all areas of response by candidates.

Candidates performed particularly well in the following questions:
- Q1 and 2(b) on logic gates and combinational logic;
- Q4 on the comparator;
- Q6 on semiconductors and MOSFET;
- Q8 on the inverting amplifier.

Lower marks were achieved in the following questions:
- Q7 on the band-pass filter;
- Q10 on slotted discs. In particular part (b)(ii) the photodiode detector circuit;
- Q11 on wireless communications;
- Q12 on communication systems.

Comments on individual questions/sections

Q.1 Straight forward and very well answered.

Q.2 Part (a) was again straight forward and well answered, part (b) was a synoptic part mostly well answered.

In part (b) it was evident whether a candidate had a broad knowledge of all elements of the course therefore producing full mark answers and those who were unprepared for the synoptic element and therefore used incorrect equations for part (i).

It is suggested that candidates learn the application of the formulae on the data sheet, in particular where frequency formulae are concerned. Thus ensuring the correct selection of formula in a question.

Q.3 Many excellent, fault free responses. Too many unnecessary errors in (b) and (c).

In part (b) many candidates worked through the Boolean algebra with confidence. However, too many were unable to progress past the application of de Morgan's theorem often due to the failure to use brackets in the algebra.

In part (c) the commonest errors involved not understanding the Karnaugh map.

Q.4 Many excellent responses.

A range of approaches were possible for part (b) all of which could lead to the correct answer. Where there were errors, these tended to be due to using the wrong resistor values in voltage divider calculations.

Q.5 Most candidate showed a good understanding of the ADC.

A surprising number of candidates were unable to identify the simplest Boolean equations in part (b), possibly because of a confusion between "simplest" and "unsimplified".

Q.6 Another very well answered question.

Candidates demonstrated an excellent understanding of MOSFETs both graphically and their application in circuits.

Q.7 There were many candidates that had difficulty with this question.

Many responses to part (a) showed that the candidate was not clear about the application of the graph to the quantities. They were therefore unable to extract the data from the graph that was required to perform the necessary calculations. Bandwidth in particular was poorly understood.

In part (b) the calculations were often well carried out. In part (i) there were errors in powers of ten and in the application of the equation. Whilst in part (ii) difficulties were with using the calculated value of R_D to find V_{OUT}.

Part (c), the QER question, had a wide range of responses. The question relied on an in-depth knowledge of the voltage follower circuit which the very best responses demonstrated clearly. However, many candidates had very limited or no knowledge of this simple yet important circuit, at best quoting some properties of the circuit but failing to explain the role of them in impedance matching.

Q.8 Well answered by the majority issues mainly arose with parts (a)(ii) and (b)(iii)

In part (a) the difficulty was in calculating the equivalent parallel resistance for the gain when the switch is closed. Ecf here was key in achieving marks in the later parts.

In part (b)(iii) some candidates tried to calculate the slew rate using the incorrect formula. It is important that candidates know the applications of formulae on the data sheet.

Q.9 Some had difficulty with the circuit diagram others with the calculation.

The multistep calculation in part (a) was tackled successfully by many. The errors that occurred in responses did so at different steps of the calculation. The commonest were mis-calculating the collector current and failing to subtract 0.7 from the voltage when calculating the voltage across the base resistor. The layout of these calculations was often poor with a lack of a logical process through what was written.

The completion of the circuit in part (b) was similarly well done by many. However, too many candidates were unable to complete elements of the circuit.

Q.10 Issues with the circuit diagram.

Part (a) was generally well attempted. The issues were almost entirely with (b)(ii), completion of the circuit was rare with most candidates achieving only 0 or 1 marks.

Q.11 Questions on wireless communications usually cause many candidates difficulty.

The biggest problem for candidates was the interpretation of the frequency modulated graph in part (b). There are examples of how to tackle this type of question in the student e-book on the WJEC website.

Part (c) was very well done by most candidates.

Q.12 Explanations need to be precise in the use of language.

The explanation in part (b)(i) caused many to lose marks due to either the imprecision of language or the lack of understanding of SNR.

A LEVEL ELECTRONICS

GCE A level

Summer 2025

Component 2 – Application of Electronics

Overview of the Component

Questions addressed all topics in the Component 2 specification, with synoptic elements of assessment in parts of questions 3, 5, 6, 7 and 8. All assessment objectives were assessed. The level of demand of the paper was comparable with that in previous years.

Overall, the standard of answers was high. A particular strength was the responses to calculations. Candidates usually included intermediate steps and evidence of knowledge of multipliers in calculation questions. Diagrams were usually accurate and well-drawn, in pencil. In both aspects, this was an improvement over previous years. Often, candidates underpinned their responses by including diagrams. While presentation was generally good it was difficult to read some candidates' handwriting.

Candidates performed particularly well in the following questions:

- Q1(c) - design of a monostable circuit, including staged development of the time period calculation;
- Q3(a) and (b) - state diagram for a sequence generator, including unused states;
- Q4(b) - completing microprocessor code for testing the minibus reversing switch;
- Q7 - the audio mixer, including calculating the output voltage for given values of input and sketching a graph of output for given input signals.

The following questions were less well answered:

- Q5(a)(iii) - calculating the number of PCM channels possible using TDM;
- Q9(b)(i) - how the voltage regulator counters the effect of a falling output voltage.

Comments on individual questions/sections

Q.1 Some candidates failed to read the questions carefully enough.

In (a), the question mentioned both pressing and releasing the switch. However, many traces ended on 12V, ignoring the release.

Part (b)(i) and (c) were examples of successful calculations, though many omitted to quote a preferred value as the answer in (b)(i) - another failure to read the question.

Q.2 Explanations were often 'woolly' and poorly thought out. In this question, examples of this were answers to (a)(iii) and to (c)(i), where few produced clear explanations of 'ripple'.

'Error-carried-forward' (ecf) produced benefits. In questions such as part (b) of this question, marks were awarded when the $\overline{Q}$ trace was drawn as the inverse of an incorrect Q trace.

Q.3 Sequence generator questions are nearly always well-answered.

Parts (a) and (b) followed this trend. However, question-reading errors surfaced when candidates failed to see, or ignored the instruction to "...complete the Karnaugh map...", instead generating Boolean expressions for the states initially given in the maps.

Part (e)(ii) generated more vague, unstructured responses. Examiners were looking for answers to address two aspects: Were there any stuck states? What is the effect of the unused states?

Q.4 Answers to part (a)(ii) often demonstrated another aspect of the failure to read the question carefully. Many candidates ignored the fact that the question flagged up the two elements needed in their answers - the effect of the instruction and why it is needed.

Part (b) was almost always answered correctly – one of the impressive features of the paper.

However, part (c), completing the instructions in lines 130 and 131 was not well-answered, revealing lack of understanding of the role and structure of the INTCON register.

Q.5 Part (a)(ii) was well-answered. In part (a)(iii), the important thing was to round down the answer to the nearest whole number of channels – a detail that most appreciated.

On the other hand, back in 'woolly' territory, there were very few convincing explanations of the effect of the Schmitt trigger in part (b)(ii). In part (b)(iii), most knew the shape of its characteristic curve, and many got it completely right.

Q.6 In part (b), many answers failed to express clearly that the advantage is to maximise the bandwidth of the preamplifier. In part (iii), section I, the calculation, was usually correct. Section II was often correct, but section III rarely so.

In part (d) (ii), the design of a treble cut filter circuit, few designs quoted resistor values as preferred values.

Part (e) was well-answered for a calculation involving logarithms and decibels. However, quite a few forgot to consider the effect of noise power.

Q.7 An excellent response - very well-answered! The biggest challenge seemed to be the output signal in (a)(ii) - inverted, sitting on a DC level of 3V with an amplitude of 10V.

Q.8 Another reading issue – part (b)(i) asks for '...component...'. Many quoted a signal, often 'V_T'.

In (b)(iii) II, there were many carefully drawn sine waves, but not many hit both targets of reduced amplitude, delayed by one 'square' on the graph paper.

Q.9 In part (a), most knew the meaning of load regulation, whereas very few answered part (i), about line regulation, correctly.

In (b)(i), there was a recurrence of the ‘woolly’ and the vague. Candidates should plan these answers, using the spare sheets at the end of the paper if necessary.

Performance in the QER question, 9(c) varied widely, as expected. Some were distracted by calculating the rms output of the transformer. Others worked back from power rating to calculate the current flowing in the zener or the resistor. A few saw a clear path, considering the voltage drop across the full-wave rectifier, obtaining the current through the 150W resistor, deducing the transistor base current and hence its collector current and finally finding the output voltage and current capability. Most knew to make suggestions for improvements, e.g. using a transistor with a greater value of current gain.

Component 3 – Extended System Design and Realisation Task

Overview of the Component

This component requires candidates to complete two tasks independently. The tasks build on the concepts studied and the requirement to relate practical circuit design and realisation to knowledge and understanding gained from the study of components 1 and 2.

Task 1 (20 marks) involves the development of a microcontroller system programmed through assembler language.
Task 2 (50 marks) is a substantial system development including analogue and digital sub-systems in an integrated design.

Each task enables learners to carry out a design and realisation task based on an individually identified problem, context or opportunity.

Centres are to be congratulated for their effort in presenting candidates' work for moderation and online recording of centre marks. Most samples were sent promptly and were well organised.

In most cases the marking criteria were understood well and applied consistently. The assessment of the work was within tolerance for the vast majority of centres but in a small number of centres, adjustments to marks were required. It was pleasing to see that some centres are actioning the advice given in their individual moderator reports. It is important that all centres do this.

Candidates should focus on a problem that will enable them to write a design specification based on a specific, identified problem. In most cases this matched the candidates' ability. Some centres clearly encouraged their higher ability candidates to produce some highly complex work. However, there were a few centres where the work was below A level standard. Also, some less able candidates attempted work that was clearly too difficult for them and often ran out of time and/or didn't finish it as a result. It is important to guide candidates to projects that will provide a level of challenge that is appropriate to their ability.

Many candidates failed to provide meaningful specifications and simply quoted power supply values, current consumption, timings, price etc. without justification. These types of parameters should not be considered a quantitative specification.

Design specifications should contain a range of both qualitative and quantitative parameters based on the analysis of the problem. Detailed, realistic, justified and measurable specifications with tolerances (where relevant) need to be included. Some of the specification points suggested did not reflect the rigour expected to justify a higher tier mark.

It is expected that students make use of their theory notes and the e-book for the NEA. Searching the internet/textbooks for basic information such as component data or pin-out diagrams for ICs is not relevant research. Some research did not address the requirements of the problem to inform the specification.

Clear photographic evidence should be submitted and the majority of centres provided excellent photographic evidence. However, some centres provided images of circuit layouts that tended to be either obscured, too small or lacking clarity to see any detail. In some instances, the accounts of system design and recording of test results were very sketchy. Further photographic evidence, for example, showing testing, together with explanations would have been beneficial to help support the assessments.

Test results obtained from circuit simulations are only valid if real components (e.g. LM741, BC548) are used rather than the generic IC1 and Q1. Real components not only model real circuit behaviour but provide an accurate high quality and fully labelled circuit diagram.

Again, the Evaluation section was a common weakness in both tasks. To access the highest level, candidates should first structure a full specification. This will then aid candidates to access the full range of marks for the evaluation as they test against their technical specification. A poor evaluation was often the consequence of having few measurable parameters in the specifications.

Improvement suggestions must be relevant and state how they would be beneficial rather than simply mentioning making it smaller, using louder buzzers or incorporating an on/off switch. Thought should be given to the improvements, since e.g. suggesting a buzzer rather than a flashing light for a system made for a deaf person is not viable!

Some centres were not using the new declaration form. As set out in a circular to all centres in January 2024, a new declaration form was introduced to include an explicit declaration in relation to the use of AI. The use of this form became mandatory for submissions for the 2025 series.

Please note that from Summer 2026, Electronics NEA will go online and samples must be uploaded electronically to IAMIS rather than posted to moderators.

Tasks
Comments on tasks/questions relating to candidate performance/meeting assessment criteria

Task 1
For the microcontroller task at A level, candidates are required to program a microcontroller using assembly language, other programming languages are not acceptable. Most candidates wrote their own assembler programs using MPLAB. However, some candidates generated their code from a flowcharting program. This is unacceptable; candidates should write their own assembler code.

Some centres did not use the template provided by Eduqas/WJEC. It is important that centres use this template. All standard sub-routines are listed in it and any subroutines called and equate statements used should be included in the task 1 template. It is important that candidates realise that these sub-routines and equate statements actually exist.

Please note that if the centre is providing its own template, then a copy of this template should be included in the report. Candidates cannot be given credit for minor alterations to delays provided on a template. Also, credit cannot be awarded for commands used to configure the ports. However, credit can be given should these same commands be used by the candidate in their main program and any subroutine they write. To gain the full range of marks in system development candidates are required to provide 10 or more different commands. Using the same command multiple times only counts as one. It is good practice to list the commands and port bits used.

Design specifications should contain at least 2 justified qualitative / quantitative parameters, with tolerances. Specifications should not make direct reference to the circuit layout or specific microcontroller pins that are to be used in their future designs.

All components must be clearly marked with the correct IC names in and not left as generic IC1 to warrant the mark for an accurate circuit diagram.

Task 2
A project should consist of block diagram showing a number of sub-systems that are then individually tested and interconnected. Signals need to be transferred from one sub-system to another as a complete system. How this occurs in terms of the function of each block needs to be explained in the ‘Evaluation’ section. A design specification that results in a solution containing several independent circuits should not be awarded marks for the complete circuit diagram. This was observed in a few centres.

A full specification should include 3 or more detailed, realistic, measurable and justified parameters with tolerances where applicable. eg if a system is to be portable, the power supply is probably going to be a pp3 9V battery, although this can be converted to another value using the necessary sub-system. This type of justification was rarely seen.

Sub-system specifications should at the very least give input and output voltages. At this level, some of the lesser sub-systems should be incorporated into a larger sub-system. For example, a light sensor (resistor and LDR) and comparator could be considered a single block that produces an output signal under certain lighting conditions. A lot of centres were observed to have candidates presenting very simple sub-systems.

In system development, candidates are required to use 6 or more different sub-systems that demonstrate a degree of complexity representative of the A-level course. More simplistic circuits cannot access the full range of marks in this section. Single components e.g. single logic gates cannot be accepted as sub-systems. Again, this was observed in many centres.

When testing sub-systems, there should be evidence of tests carried out on the actual components used in the final design rather than generic simulation models, a lot of centres provided good photographic evidence of this, whilst a minority only showed simulations.

Often, marks were awarded for alternative sub-system development with very little evidence of investigating them. Candidates are required to give thorough reasons for their final sub-system choice after investigating alternative circuits in at least 3 cases.

There was often little analysis or tabulated results, although measurements had been taken as evidenced in photographs. It is important to compare results with specifications and their tolerances and comment on this rather than simply stating “the specification has been achieved”.

The physical circuit layout produced by most candidates was of a very good standard, with the majority of circuits constructed very neatly on breadboard with horizontal and vertical wires not covering ICs or other components.

Task marking
Comments on approaches to internal marking

A large number of centres showed little indication on the mark schemes in either task, as to why marks were allocated and some did not show marks at the end of each section. It is good practice to indicate where (and possibly why) marks have been given (or not) and also reference it on the candidates’ work. This not only helps the moderation process but also benefits candidates by illustrating how and where they have achieved the criteria. For those centres that did annotate candidates’ work and mark schemes it was a great help in moderation.

Candidates are not required to satisfy every individual bullet point within an assessment tier to access the marks. A holistic approach is taken when assessing these tiers; if a candidate has produced a circuit that worked consistently and reliably but has not recorded all of their testing, credit can still be given for this point. Further teacher annotation on the scripts as to where a circuit has been witnessed as working or where testing has been carried out would aid the moderation process.

The range of tasks produced within most centres was very good. In some centres, candidates produced a very good range of tasks with some of the work being outstanding and demonstrating considerable innovation. In a small number of centres all candidates produced similar or very simple projects.

It was also evident that some centres had prescribed possible tasks. Candidates should select their own focus for the tasks based on different, individual problems or interests and this is expected to produce a wide range of tasks within a centre. Candidates should focus on a specific problem to analyse that enables them to research and write a design specification based on their identified problem

Supporting you

Useful contacts and links

Our friendly subject team is on hand to support you between 8.30am and 5.00pm, Monday to Friday.
Tel: 029 2240 4254
Email: electronics@eduqas.co.uk
Qualification webpage: AS/A Level Electronics

See other useful contacts here: Useful Contacts | Eduqas

CPD Training / Professional Learning

Access our popular, free online CPD/PL courses to receive exam feedback and put questions to our subject team, and attend one of our face-to-face events, focused on enhancing teaching and learning, providing practical classroom ideas and developing understanding of marking and assessment.

Please find details for all our courses here: https://www.eduqas.co.uk/home/professional-learning/

Regional Rep Team

Our regional team covers all areas of England and can provide face-to-face and online advice at a time which is convenient to you.

Get in contact today and discover how our team can support you and your students.
Regional Support Team | Eduqas

Eduqas Qualifications

We are one the largest providers of qualifications for schools, academies, sixth form and further education colleges across England, offering valued qualifications to suit a range of abilities. Each and every one of our qualifications is carefully designed to engage students and to equip them for the next stage of their lives.

We support our education communities by providing trusted qualifications and specialist support, to allow our students the opportunity to reach their full potential.

WJEC
245 Western Avenue
Cardiff CF5 2YX
Tel No 029 2026 5000
Fax 029 2057 5994
E-mail: exams@wjec.co.uk
website: www.wjec.co.uk