

GCSE Examiners' Report

Electronics

GCSE

Summer 2025

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Introduction

Our Principal Examiners' report provides valuable feedback on the recent assessment series. It has been written by our Principal Examiners and Principal Moderators after the completion of marking and moderation, and details how candidates have performed in each component.

This report opens with a summary of candidates' performance, including the assessment objectives/skills/topics/themes being tested, and highlights the characteristics of successful performance and where performance could be improved. It then looks in detail at each unit, pinpointing aspects that proved challenging to some candidates and suggesting some reasons as to why that might be.¹

The information found in this report provides valuable insight for practitioners to support their teaching and learning activity. We would also encourage practitioners to share this document – in its entirety or in part – with their learners to help with exam preparation, to understand how to avoid pitfalls and to add to their revision toolbox.

Further support

Document	Description	Link
Professional Learning / CPD	Eduqas offers an extensive programme of online and face-to-face Professional Learning events. Access interactive feedback, review example candidate responses, gain practical ideas for the classroom and put questions to our dedicated team by registering for one of our events here.	https://www.eduqas.co.uk/home/professional-learning/
Past papers	Access the bank of past papers for this qualification, including the most recent assessments. Please note that we do not make past papers available on the public website until 12 months after the examination.	Portal by WJEC or on the Eduqas subject page
Grade boundary information	<p>Grade boundaries are the minimum number of marks needed to achieve each grade.</p> <p>For unitised specifications grade boundaries are expressed on a Uniform Mark Scale (UMS). UMS grade boundaries remain the same every year as the range of UMS mark percentages allocated to a particular grade does not change. UMS grade boundaries are published at overall subject and component level.</p> <p>For linear specifications, a single grade is awarded for the subject, rather than for each component that contributes towards the overall grade. Grade boundaries are published on results day.</p>	<p>For unitised specifications click here:</p> <p>Results and Grade Boundaries and PRS (eduqas.co.uk)</p>

¹ Please note that where overall performance on a question/question part was considered good, with no particular areas to highlight, these questions have not been included in the report.

Exam Results Analysis	Eduqas provides information to examination centres via the WJEC Portal. This is restricted to centre staff only. Access is granted to centre staff by the Examinations Officer at the centre.	Portal by WJEC
Classroom Resources	Access our extensive range of FREE classroom resources, including blended learning materials, exam walk-throughs and knowledge organisers to support teaching and learning.	https://resources.eduqas.co.uk/
Bank of Professional Learning materials	Access our bank of Professional Learning materials from previous events from our secure website and additional pre-recorded materials available in the public domain.	Portal by WJEC or on the Eduqas subject page.
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Executive Summary

Candidates' performance in GCSE Electronics this year was better than in previous years. The mean marks for both Component 1 and 2 exams were significantly higher than in 2024. The mean mark for Component 3 (NEA) was slightly higher than 2024.

Analysis of responses to questions showed the level of difficulty of the Component 1 and 2 exams to be slightly lower than 2024 and closer to the 2023 level.

Component 1 & 2 exams

Both exams had questions covered all parts of the specification, including some synoptic questions. Candidate performance was good overall, with some achieving excellent marks across the range of topics. Candidates attempted the majority of questions. The mean mark in Component 2 was less than in Component 1. This is usually the case, reflecting the more applied nature of questions in this paper. However some candidates achieved excellent marks in Component 2.

In Component 1, candidates achieved highest marks in questions on circuit analysis, logic gates, sensing circuits and MOSFETs. In Component 2 the highest marks were achieved on interpretation of an oscilloscope trace, 555 timers and inverting amplifiers.

The QER question, particularly in Component 1 this year, was the most often omitted and candidates scored fewest marks on this question. Component 1 topics in which candidate scored lowest marks were block system design, logic circuit design and NAND gate implementation. In Component 2 the lowest marks were achieved in non-inverting amplifiers, D-type flip flops and 555 astable circuits. Quality of presentation by some candidates was poorer than previous years.

The GCSE Electronics eBook includes examples and exercises on all topics. This and other resources are available on the [GCSE Electronics resources webpage](#).

Component 3 NEA

As in previous years, work presented for moderation was well organised. Work was accurately marked by most centres, with only a small number of centres' marks requiring adjustment

Examples were seen of well-planned and developed circuits. Many physical circuits were well constructed, neatly laid out and thoroughly tested. Good photographic evidence of the stages of development and final circuit were provided. In a minority of reports, photographs were too small or unclear for details to be legible.

Most centres provided clear annotation of candidates work which is helpful for moderation. From summer 2026 NEA samples must be uploaded electronically and will be moderated online. Clear annotation on the mark scheme, showing the criteria achieved and marks awarded will be particularly helpful.

NEA requirements are generally well understood. A good range of projects were produced by most centres however in some centres, candidates' work was focused on a common theme. Candidates' work must be based on an individually identified problem.

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Component 1 – Discovering Electronics

Overview of the Component

This component is aimed at testing the fundamental concepts of Electronics and is broken down into small parts to test multiple factors of a candidates' knowledge of the essential topics needed to make progress in the subject.

Candidate performance in this component was good overall with some excellent answers being observed across the whole range of questions.

There were a small minority of candidates that achieved very few marks as much of their scripts were blank leaving nothing for markers to attribute any marks to. In contrast a small number of candidates achieved near full marks.

The question paper was broken down into 44% (AO1), 44% (AO2) and 12% (AO3).

The topics tested were

1. Basic Logic Gates / Truth Tables / Boolean Identities.
2. Interpretation of Truth Tables / Logic Circuit Design / Conversion of logic circuits to NAND gates.
3. Use of Ohm's Law and Resistor Colour Code / Circuit Voltage / Current rules.
4. System design using a functional block approach.
5. Regulated Power Supplies
6. Sensing Circuits using Operational Amplifier
7. Half-wave Rectification
8. Transistor Switching Circuits

Question 4 was a synoptic question, requiring knowledge from Component 2.

The overall performance on the paper was good with an overall mean mark of 58.1 for matched candidates which is an increase on previous years. Across all candidates, marks ranged from 2 to 80.

In general candidates attempted the majority of questions. The most successful question was the circuit analysis question which has proved in previous years to be quite difficult. The mean mark for this question was 14/17 which shows a big turnaround from previous years. Questions on logic gates, sensing circuits and MOSFETs were also answered well.

In contrast the QER question was the least successful on the paper with over 100 candidates omitting the question completely. The question tested the ability of candidates to analyse and evaluate a circuit design and communicate their understanding in extended prose. Candidates had to determine if the provided circuit design was suitable and despite having two possible routes to work through it proved to be challenging. A large number seemed overly concerned with adding a reverse bias diode around the lamp to protect the transistor. Candidates should be aware that the diode is only required with electromagnetic devices. e.g. relays, solenoids and motors. Other topics in which candidate scored lower marks were block system design, logic circuit design and NAND gate implementation

The quality of presentation in a number of candidates' answers was poor compared to previous years, for example, diagrams drawn in ink instead of pencil with multiple crossing out. No attempt to redraw a messy diagram on the spare pages made it very difficult to award marks on a few occasions. The use of a ruler was sparse and when it was used candidates were unable to follow graph paper grids accurately. There seems to be an increase in the number of candidates using word-processors to prepare the answers. Given that this is their normal way of working they should be able to use an equation editor to lay out mathematical solutions clearly.

Comments on individual questions/sections

1. A successful question for the majority of candidates. A few lost marks in part (b) for not recognising that the NAND gate was actually configured as a NOT gate, and giving the X output as that of a NAND gate even though there is no connection from input B. The Boolean identities were correctly answer in the majority of cases.
2. A number of candidates struggled with the identification of standard Logic Gates from the truth table which resulted in difficulties drawing the logic circuit. A number of candidates use a NAND gate in the circuit despite the instruction to only use AND, OR and NOT gates. Several candidates did not know the NAND equivalent circuits for standard Logic gates making identification of double inversions impossible.
3. Circuit rules for voltage and current are still not well understood by a large number of candidates. Many candidates mixed up the relevant units Volts, Amps and Ohms for basic circuit parameters. The Resistor Colour Code was well understood.
4. A number of candidates seemed to be unaware of the function of the given functional blocks. This may be due to the long period of time elapsed since covering the block diagram approach, but sorting these into input / processing / output was poor. This lead to further difficulties in constructing a working block diagram to meet the specification. There were far too many examples of complete randomisation of blocks placed into the diagram, for example the pulse generator was often seen despite there being nothing in the specification that would require its use. The synoptic element which required the knowledge of the block diagrams for a simple PA system and use of a mixer to combine inputs was answered poorly by in the majority of candidates.
5. The basic operation of the zener diode to produce a regulated voltage is not understood by a number of candidates. As this is the main source of providing a regulated voltage supply at this level, there are clear misunderstandings about this particular circuit, especially relating to the effect of increasing the input voltage having no effect on the voltage across the zener diode.

6. Candidates found the comparator design quite straightforward this year, although there are a number that did not know the correct symbol for a thermistor. Only a minority were unable to get the orientation of the resistor and thermistor correct. There were a number of candidates that were unable to manipulate the MOSFET formula without making fundamental arithmetic errors.
7. The number of candidates that were unable to complete the diagram for a half-wave rectifier was quite surprising, as only a diode was needed. Quite a number left this part completely blank. More surprising was the number of candidates that gave C and D as the expected outputs from the half-wave rectifier.
8. The transistor switch is still not well understood by a large number of candidates. There were two possible routes to the solution of this question, Either to work backwards from the current needed to light the lamp, dividing by gain of transistor to get base current, and hence show that V_{IN} was insufficient. Alternatively they could start with V_{IN} and show that the base current even when amplified by the transistor would be insufficient to run the lamp at it full rated power.

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Component 2 – Application of Electronics

Overview of the Component

This component is aimed at testing the application of electronics in larger systems and requires candidates to apply the knowledge gained about basic building blocks and apply this to their function in a larger system.

Candidate performance in this component was lower than that in Component 1 reflecting the fact that this paper is based more on application to whole systems rather than straight recall questions. A number of low marks were observed, however there were still a number of excellent answers across the whole range of questions.

The question paper was broken down into 44% (AO1), 44% (AO2) and 12% (AO3).

The topics tested were

1. 555 Astable Circuits.
2. Use of an oscilloscope to determine amplitude, period and frequency of an astable circuit.
3. 555 Monostable circuits / Resistors in series / Selection from E24 series.
4. Inverting amplifiers.
5. Operation of Decade Counter / Automated sequence generators.
6. Applications of D-Type flip-flops.
7. Non-inverting Amplifier
8. Flowcharts as part of larger control system.

Question 3 and 5 were synoptic questions, requiring knowledge from Component 1.

The overall performance of the paper was good with an overall mean mark of 57.4 for matched candidates which is an increase on previous years and slightly below the mean of 58.1 for Component 1. Traditionally the Component 2 mean has been much lower than Component 1 due to the much higher demand of dealing with large systems requiring application of understanding rather than straight recall. Part of the reason for this increase is the comparative performance in the QER questions over the two papers. In Component 2, far more candidates attempted and scored higher marks on the QER question than the same type of question in Component 1.

There was a consistent attempt rate at all questions and there was no question that proved significantly easier or more difficult across the paper with the facility factors being very close.

The question showing greatest success was the reading and interpretation of the oscilloscope trace. Other questions answered well were on topics such as 555 monostable and inverting amplifier.

The least success was achieved in the question requiring the design of a non-inverting amplifier. Other topics answered poorly were D-type flip flops and 555 astable circuits. Despite this, across all candidates marks ranged from 0 to 80

The quality of presentation in some candidates answers continues to be poor compared to previous years as in Component 1. As mentioned for Component 1 an increase in the use of word processors is being observed yet the need for an equation editor is even more important in this component due to the increase of quite complex formulae.

Comments on individual questions/sections

1. The two equations needed to answer each part of this question were on the facing page, yet despite this many candidates copied the equations incorrectly, or left the questions blank, losing a significant number of marks.
2. Some candidates were unable to interpret the oscilloscope trace correctly. There was confusion over the amplitude measurement once again even though this has been clarified many times. Candidates were also confused about what units to give their answers for amplitude (V) and period (ms). This misunderstanding in units led to the incorrect frequency being obtained by the candidates.
3. A significant number of candidates were unable to complete the trigger circuit correctly. Many of them tried to use the changeover part of S_1 in the trigger circuit showing a misunderstanding of the changeover switch and the specification which states that the timer has two modes of operation. Most candidates could identify two resistors that could be used to make the $124k\Omega$. A minority of candidates made complex parallel and series circuits with multiple resistors ignoring the requirement to use just two resistors. Most candidates were able to select the appropriate formula for a 555 monostable and determine the minimum time delay. In the attempt to determine the value of the resistor for a 7 minute delay a number of candidates found it hard to manipulate the formula to obtain a value for R_2 .
4. Generally answered well but a large number of candidates omitted the fact that the output wave was clipped at $\pm 10V$.
5. When attempted, this question was answered well and the candidates showed a good understanding of the decade counter. Most common errors were neglecting the reset occurring on pulse 7 so the outputs revert to those at clock pulse 0. There were a number of candidates who indicated that the counter stopped at this point. For the system design in part (b) candidates struggled to get the two Boolean expressions needed for the blue output joined by an OR statement, most candidates stopped with one and therefore lost some marks here, and in the final part of the question.
6. The understanding of the two bit counter was disappointing with candidates struggling to complete both the state of the LED table and expected frequency of each LED. In contrast candidates completed the combinational lock application very well. Poor drawing let the majority down when adding a MOSFET to the final part of the question, especially the symbol for a MOSFET which was poor.

7. The main issues in this question were caused by poor drawing skills in (a) and (c), too many candidates using ink instead of pencil and then having to make significant crossing out when realising that a mistake has been made.
8. No specific issues to highlight, candidates found the flowchart based QER quite accessible and the majority were able to make some inroads into the question and provide some suggestions for how to improve the program.

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Component 3 – Extended System Design and Realisation Task

Overview of the Component

The NEA is an integral part of the WJEC Eduqas GCSE in Electronics. This component requires each learner to produce a single extended system design and realisation task independently. Building on the systems developed throughout the specification and the requirement to relate practical circuit design and construction to knowledge and understanding within Components 1 and 2.

Centres must be praised for their effort in presenting candidates' work for moderation, and for recording the marks online.

The assessment of the work was within tolerance for most centres this year, but in some centres adjustments to marks were required.

Comments on individual questions/sections

Some centres used the wrong candidate declaration form. As set out in a circular to all centres in January 2024, a new declaration form was introduced to include an explicit declaration in relation to the use of AI. The use of this form became mandatory for submissions for the 2025 series.

Most centres provide annotation of candidates work. Centres that did not provide annotation this year should consider providing an indication on the mark scheme of which level descriptors were achieved when Electronics NEA goes online in 2026. This would be very helpful in justifying marks awarded by the centre during the moderation process.

The candidates of most centres produced a very good range of projects. However, in some centres many candidates' work seems to have focused on a common theme. Candidates should focus on their individually identified problem to enable them to write a design specification.

Most centres provided excellent photographic evidence of the candidates' testing and circuits. In a minority of reports, photographs were too small or unclear for details to be legible.

System Planning

Design specifications should contain a range of both qualitative and quantitative terms based on their analysis of the problem. To access the higher band, the specification should contain detailed measurable electronic parameters. Examples amongst many acceptable measurable parameters this year included the temperature at which the circuit activates, the time duration for circuits to be active, the required frequency for system to be random and the number at which a counting system should reset.

Unless very good reasons are provided as justification, neither the battery supply voltage nor the number of components should be considered as quantitative specifications.

System Development

Candidates of many centres this year showed a high standard of rigorous sub-system testing. These centres set up their sub-systems on breadboard and showed excellent photographic evidence of the test instruments in use. The results were then analysed logically.

Sub-systems should be constructed and tested individually during development of the system, in order, rather than testing each sub-system of the fully assembled final circuit retrospectively.

Centres that choose to carry out tests on circuit simulations should note that results are only valid if the actual components such as BC108 or 2N5060 are used in the circuit are tested. This means that test results obtained using ideal generic components such as IC1 and Q1 should not be credited as valid tests. .

Awarding accurate marks is critical to ensure that candidates receive fair and consistent reward for the work produced. Banded mark descriptors help to determine the correct band where a candidate's work fits. Some centres awarded top band marks for development when there were less than five different sub-systems developed. Testing two very similar sub-systems such as a red LED and a green LED as outputs should not be credited as two separate tests. Some centres also credited single components as sub-systems. For example, input switches and a logic gate should be considered as one sub-system rather than two.

For each sub-system a test reading should be provided with the output activated and non-activated.

When using a flowchart program, the flowchart itself should be tested as one sub-system. Four other electronic sub-systems are required for top band marks. For the flowchart sub-system testing, simulation tests should be carried out for the program and include screenshots of the results.

System Realisation

Centres generally either produced their circuits on PCB or on breadboard. If candidates produce the final circuit on PCB, then layout diagrams showing their modifications to the software generated layouts must be included. Similarly, either a clear photo, or a diagram of the plan layout should be included for a breadboard.

To gain the full range of marks for system realisation candidates must have a very well organised physical circuit layout (rather than a circuit diagram), with wires and components arranged vertically/horizontally to a high standard.

As was the case with sub-system testing, many centres this year showed a high standard of final circuit testing using appropriate test equipment and included clear photographic evidence of the actual testing taking place. They demonstrated in depth analysis and comparison of their numerical results with their quantitative specifications.

The majority of candidates provided excellent photographic evidence showing their final circuits in operation. This was an effective way of demonstrating their circuits working reliably.

Some of the testing however, tended to be observational with limited use of test equipment. The recording of test results tended to lack detail and the analysis of the results was superficial. Marks were sometimes awarded for reliable operation of 3 sub-systems when glaring errors could be seen in the circuits.

Evaluation

Good practice evaluations made valid, critical and objective evaluations of performance against measurable numerical electronic design parameters in the specifications. So the evaluations should compare measured values obtained during the final full circuit testing against the measurable parameters in the specification. For example the design specification temperature switching threshold (with tolerance if applicable) should be compared with the actual value measured in the final physical circuit.

Many centres over awarded marks in this category because the original specification did not have realistic measurable parameters. This resulted in simplistic evaluations.

Many candidates made sensible, realistic suggestions for improvements, with explanations. To access the higher band, candidates must explain how their suggestions would lead to improvements.

Supporting you

Useful contacts and links

Our friendly subject team is on hand to support you between 8.30am and 5.00pm, Monday to Friday.

Tel: **029 2240 4254**

Email: electronics@edugas.co.uk

Qualification webpage: [GCSE Electronics | Edugas](#)

See other useful contacts here: [Useful Contacts | Edugas](#)

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