GCE A LEVEL EXAMINERS' REPORTS

A LEVEL (NEW)
ELECTRONICS

SUMMER 2019

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ELECTRONICS

GCE A LEVEL (NEW)

Summer 2019

COMPONENT 1: PRINCIPLES OF ELECTRONICS

General Comments

Candidates should always be encouraged by their teachers to show stages in working that lead to the final answer. Should they make a mistake and not obtain the correct answer, they can gain credit for the intermediate steps. An incorrect answer, unsubstantiated, gains no marks.

On the whole, calculation questions were well-answered. However, it appeared that candidates some candidates did not really understanding what they were calculating.

Candidates must always read the question carefully. In particular, they must identify the type of question and distinguish between the verbs ‘explain’ ‘describe’ and ‘state’ to establish what kind of answer is expected.

Comments on individual questions/sections

Q.1 (a) (i) Both $\overline{(A+B)}$ and $\overline{A} \,.\, \overline{B}$ were accepted as correct answers. Some candidates confused the NOR function with NAND.

(ii) The circuit symbol required was usually correct, though some drawings were so poor that they looked like (and possibly were) NAND gates. Some had only two inputs while others had four.

(iii) The graph for output Q was usually correct. Some were drawn freehand often leading to mistakes.

(b) (i) The task was well-understood and implemented. For some, ‘e.c.f’ , usually on the Z column, avoided what would otherwise have been a low mark.

(ii) Few candidates drew NAND gates with inputs joined together for both the two-input gates as well as for NOT gate equivalents, and lost a mark.

(iii) Most candidates correctly identified the redundant NAND gates.

(iv) The majority of candidates forgot to label the ‘Select’ inputs with ‘C’,’B’ and ‘A’.

Q.2 (a) Many provided the answer with no supporting working. Striking errors included “$A \,.\, \overline{A} = 1$”.

(b) Answers were usually correct but there were numerous instances of $\overline{(C+B+A)}$.

(c) Most candidates obtained the correct Boolean expression, though some were not able to complete the Karnaugh map and lost all marks.

(d) The QER question produced answers having a wide range of validity. The most obvious feature was the difference in the levels of structured approach. The best answers showed a logical and systematic approach. The majority failed to see that the NAND gate would keep the LED lit continuously when only one switch was pressed as well as when both were open.

The other aspect, the LED pulsing at 1 Hz when only one switch was pressed, was tackled more successfully, with either a ‘divide-by-two’ subsystem or a second pulse generator with a 1 Hz output frequency. Quite a few candidates worried (unnecessarily) about propagation delay, which would not cause any problems in this situation. Others wanted to reduce the system to one using only NAND gates, a step with unlikely benefits in this case.

Q.3 (a) (i) Answers that suggested that the difference was down to the need for a power supply, or not, were not accepted. Sloppy language such as “Active filters have a gain greater than 1. Passive filters don’t” or “Passive filters have a gain of 1, active filters have a gain greater than 1.” gained only partial credit.

(ii) Most candidates scored full marks, but only if the answer had a single spike with no other markings.

(b) (i) A minority confused the answer with the capacitor reactance graph.

(ii) I. Answers were usually correct, though some misunderstood, or forgot to include the multipliers.

II. The task amounted to writing down the same value as that calculated in (I). Some performed a separate calculation.

(iii) The calculations were almost always correct. There were the odd mistakes with multipliers. Some used dynamic resistance, R_D, in (II) instead of inductor resistance, r_L.

Q.4 (a) The response to this part was very disappointing. About half the answers were incorrect. The candidates seemed to lack the knowledge of how to obtain the bandwidth from a frequency response graph.

(b) (i) A sizeable minority thought the input impedance was infinite - true for the ideal op-amp, but not for an inverting amplifier.

(ii) This was usually well-answered. Some offered an answer of +/- 0.4 V.

(iii) Even though the saturation voltage was given as 12 V, many chose 10 V instead. Though the circuit was recognised as an inverting amplifier, many answers were not inverted. Some showed no effect of slew-rate at all.

(c) The characteristic curve is clearly that of a non-inverting amplifier. Some candidates, however, produced inverting amplifier circuits. Some circuits were very confused and badly drawn.

Q.5 (a) Not many understood the significance of ‘open-loop’. Many thought that it meant that there was no load attached to the output of the op-amp.

(b) (i) This produced a variety of weird symbols for the LDR - not acceptable at A-level. The orientation of the sensing unit was often wrong. Some even attached it to the output of the comparator.

(ii) Answers were usually correct. Some chose 6V (and received no marks) or 4V (which earned one mark).

(iii) There were very few correct answers here. Many decided that it meant that no current flowed from input to output.

(c) (i) The majority of answers were correct.

(ii) The same was true here. Examiners accepted the answer of $B \cdot \overline{A}$, and allowed ‘ecf’ from part (i).

(iii) Most answered this part correctly.

(d) (i) The answer ‘8’ occurred more often than the correct answer ‘2^8’.

(ii) Answers to this part were usually correct, regardless of the answer to (i).

Q.6 Answers to parts (a) and (b) were often ‘fuzzy’.

(a) There should have been two parts to the answer - 1. the problem - 2. its cause. Many answers contained only one of these. As mentioned at the beginning of the report, candidates need to understand what the questions are looking for. It is wrong to say that “… more than one-bit changes at the same time…” If so, there would not be a problem. Some emphasised “reflective” and based their answers around reflection.

(b) (i) More vague answers. For example, “Only one-bit changes at a time…” (with no mention of rotating from one segment to the next.)

(ii) Answers were rarely correct. Credit was given where only one bit changed between segments. All too often, candidates used pen to produce the diagram and then tried to change it. The result was invariably an indistinct mess. Candidates need to use a pencil and eraser for such tasks.

(c) In both parts of this question, the vast majority scored full marks.

Q.7 (a) (i) Answers produced a host of variations hinting at the word ‘bridge’.

(ii) Most candidates produced correct answers, though some with very little working. Answers with a minus sign lost a mark.

(b) All of part (b) was not well-answered.

(i) Many answers were vague and hinted at the effects of increased resistance, rather than electrical noise.

(ii) Many answers to this part made no reference to the difference amplifier.

(iii) Many candidates used inverting amplifiers or circuits with three resistors. Calculations often lacked systematic, coherent order.

Q.8 (a) (i) Some assumed 'noise' meant sounds. About half scored one or more marks.

(ii) Good answers included 'lightning' 'crosstalk with neighbouring wiring' and 'power supply'. Poor answers included 'neighbours.'

(iii) Answers were usually correct.

(b) Again, answers were usually correct.

(c) Answers were almost always correct.

(d) (i) Some tried to rejig the words 'time-division multiplexing', usually unsuccessfully. Some answers failed to go far enough. Needed the idea of time slots and taking turns.

(ii) Answers such as 'more efficient', 'cheaper', 'faster' should have been expanded.

Q.9 (a) There were few correct answers to this question which required straight forward knowledge recall.

(b) Answers needed to imply the effect of the input current/voltage on output current/voltage.

(c) (i) Some correct answers but many candidates subtracted (3 x 2.5 V) from 12 V, or subtracted a further 0.7 V. Some used Ohm's law to calculate the 'resistance' of a LED'. Some chose the smaller nearest E24 value, while others used the E12 series.

(ii) Most performed a successful current gain calculation, though some in the wrong direction, assuming that 5 mA was the collector current. Many commented that the current would be too small. The best answers went on to describe the effect on the LEDs or to say how to correct the problem.

(d) (i) Many offered answers such as "It is voltage-controlled" Very few raised the issue of protection against over-heating.

(ii) MOSFET symbols were often badly drawn loosing marks.

(iii) I. Often correctly answered. Some struggled to calculate the drain current, I_D.

II. Many answered this correctly. Some benefitted from ecf, for the drain current in part I.

Q.10 (a) Light does not travel faster or further than microwaves. Although the question does not mention fibre optic cable, some incorporated it into an answer such as “Microwaves cannot travel down an optical fibre.” Security was rarely mentioned but some said that a modulated light beam was immune to electrical noise.

(b) Answers were usually very confused. They hinted at appropriate knowledge but could not express it effectively.

(c) (i) Answers were often correct or showed enough evidence to allow the award one mark for ‘correct use of formula’.

(ii) The same was true here. Examiners allowed ecf for the frequency from (i).

(iii) This topic was not well-understood. Many answered “4 V”.

(iv) Another topic rarely understood. “Distortion” not accepted without more explanation implying loss of signal information.

(d) (i) Answers were usually correct.

(ii) Answers were usually correct.

Summary of key points

- Candidates must read the question carefully, paying particular attention to the verb: “Describe…” / “Explain…” / “State…” etc.
- Candidates should use a pencil and ruler for all diagrams.
- Candidates should practice writing answers that explain complex concepts. In the examination, they should think about, and plan their answer before they commit it to paper.
- Candidates must be able to expand multipliers.

ELECTRONICS

GCE A LEVEL (NEW)

Summer 2019

COMPONENT 2: APPLICATION OF ELECTRONICS

General Comments

There were a number of instances where candidates wrote down incorrect answers in calculation questions. They provided no indication of the steps that led to that answer and so received no marks. Had they shown the stages leading to that incorrect answer, they could have gained some credit.

Candidates are expected to be able to develop coherent, structured answers to demonstrate their understanding. This requires practice. In particular, they must mould answers to satisfy the requirements of the question, taking care to distinguish between 'explain' 'describe' and 'state', in the stem of the question.

Comments on individual questions/sections

Q.1 (a) (i) Most candidates answered this successfully. Some incorrect answers gained credit for evidence of recognising how many states in the main sequence or of using period.

(ii) Some answers referred to only one of the two states. The question asked that they "…explain the difference…" That required a discussion of both types of state.

(b) (i) Again, most answers were correct. A minority misunderstood the information contained in the table.

(c) (i) There were a few errors, particularly with the expression for D_C where some tried to use a form of $\overline{D}_A$.

(ii) Poor responses to this question on the EXOR gate.

Q.2 (a) Parts (i) and (ii) were rarely answered correctly. Many wanted the CPU to have one of the roles.

(b) (i) Many answers were correct. Mistakes were usually the syntax for instructions, e.g. 'PORTA,0' where candidates wanted to use the b'00000000' notation.
(They lost only one mark if they used it again in the third instruction, though often the wrong binary number was used, usually b'00000010'.) Some used the wrong label in the final 'goto' instruction, usually 'START'.

(ii) I. Three marks reflected the three steps:

- identify PORT B;
- translate the decimal number '5' in 'movlw d'5'' as b'00000101';

- identify bits 0 and 2 as connected to the LEDs.

Some answers were very close but then interpreted the information as bits 1 and 3 instead.

II. The first word of the question is “Why…” Instead of answering this, many translated the instructions without saying why they were needed.

III. Most answers were correct.

(c) (i) Candidates should have seen that there were two parts needed to their answer. First of all, why use an interrupt. Secondly, why not use polling.

(ii) Some diagrams had added clutter - PSU connections / LEDs / etc. Nevertheless, where they showed a switch unit (switch in series with a resistor) connected to pin 6, they received full marks.

Q.3 (a) (i) Quite a few candidates succeeded completely. Some fell at one of the last hurdles. Either they forgot to calculate the overall gain of the preamplifier (626), or they divided the gain-bandwidth product by the full gain instead of by the gain of a single stage (26). Quite a few thought that they were dealing with an inverting amplifier, but gained some credit through ‘ecf’.

(ii) Many correct answers but some odd answers such as “…to smooth the output…”.

(b) (i) Some answers were based on the wrong type of filter. Others lost marks either for misreading the log scale and choosing a gain of 3 rather than 2 for the high frequency section, or for drawing the 45^0 section, below 200 Hz, badly. Some graphs were drawn poorly freehand.

(ii) A mixed response. Many correct answers, but quite a few incorrect circuits.

(c) The QER question. Most candidates made some sensible comments on the validity of the design. However, some focussed on the “’’’input impedance…>10 kΩ …” and either misread it as <10 kΩ or =10 kΩ and so came to incorrect conclusions. A common recommendation was to change the variable resistors to a value of 135 kΩ. While this then met the requirement for voltage gain, it is an unrealistic. A value of 200 kΩ would have done the job equally well. Erroneous answers included those that treated the channel 1 and 2 resistances as connected in parallel.

Q.4 (a) (i) The majority calculated time constant successfully. A few used the formula ‘1.1 x R x C’.

(ii) Again, mostly well answered. Most recognised that it was a half-life calculation.

(b) (i) Most candidates scored at least one mark, usually for connecting a NOT gate to the output of the sub-system. Many then connected the buzzer from the output of the NOT gate to 0 V, reversing the behaviour of the system.

(ii) Very few candidates scored full marks. Some recognised that the buzzer would sound for five seconds while the door is open. Others realised that the sub-system in part (i) would sound the buzzer for three seconds. Not many added those times together.

(c) The majority scored highly on both parts (i) and (ii) of this question. A few had problems with multipliers in (i), omitting the 10^3 for kilohms. The problems resulting, when trying to sketch the output waveform in (ii), should have alerted them to an error in their frequency calculation. One unfortunate tendency in part (i) was to quote the number ‘2’ for the mark:space ratio. That answer is not a ratio.

Q.5 (a) The calculations in part (a) were usually carried out successfully. In part (iii), a few subtracted 0.7 V from the r.m.s. value of V_{SEC} instead of the peak value.

In part (ii), some drew, or attempted to draw the full-wave rectified power supply circuit. Where the circuit was correct, they lost only one mark, for incorrect rectifier connections. Where they went on to subtract 1.4 V from the peak value of V_{SEC}, in (iii), they were awarded the mark for ecf.

Part (v), the graph should have included the rectified waveform from the circuit in (ii), modified by the ripple voltage calculated in (iv). Very often, candidates offered roughly drawn signals that lacked some of that information.

(b) (i) Most completed the definition of line regulation correctly, but there were vague references to changing the load in the definition for load regulation.

(ii) The majority identified the equation correctly.

(iii) This was not well-answered. There needed to be a recognition that the voltage across the zener diode remained steady when the supply voltage changed, and a link explaining how this kept the output voltage constant. Often, the answer sounded more like an explanation of load regulation than line regulation.

(iv) About half of the candidates calculated maximum and minimum values of output voltage correctly. Others were floundering with incorrrect formulae, unsubstantiated calculations and an overwhelming desire to subtract 0.7 V from something.

Q.6 (a) Candidates should have recognised that the requirements for conduction are forward bias and a positive voltage applied to the gate, i.e. options C and E. Most identified only one of these.

(b) (i) Information about the holding current is a red-herring. The voltage across the resistor is a maximum of (24-1.2) V, to allow at least 1.2V at the gate terminal.

The minimum gate current (through the resistor) is 100 mA. Combining these, using the Ohm's law formula, gives a maximum resistance of 228 Ω.

(ii) The question asked for information about both switches and about the thyristor. Few gave complete answers. Many answers simply translated into words the information given in the graphs. "At 2 s, the voltage at both P and Q is 24 V." There was no attempt to deduce the state of the switches and thyristor. There was widespread use of the word 'activated'. This does not have a clear meaning in this situation. It was pleasing to see recognition that, at 10 s, the thyristor was reverse-biased and so switched off.

(c) (i) Most correctly identified X as a diac. Stating its function attracted some indistinct answers, such as "…improves switching…", and "…allows conduction in both directions…". Faster switching and identical conduction in both directions would both have been valid answers.

(ii) Most scored full marks on this question. Those who chose the lamp as their answer in part I were allowd ecf in answering part II.

Q.7 (a) Answers were usually correct. A few were not sufficiently accurate, particularly the amplitude of the third pulse.

(b) A recall question, this caused problems for many candidates.

(c) (i) The same was true here. The common mistake was in identifying the least and most significant bits of the output, though a mistake here allowed use of ecf in (ii).

(ii) Even with the benefit of ecf, this was not well-answered.

Q.8 (a) (i) Too many vague answers. Candidates need to practisethis type of explanation question.

(ii) Despite its prominence in the stem of the question, some managed to disregard the information that the counter is falling-edge triggered. Many scored full marks.

(b) Many failed to recognise the conditions leading to reset, or what that would mean. Many added an extra 0,0,0 row to the truth table. few scored full marks.

Q.9 (a) Many calculated overall gain and output power successfully in parts (i) and (ii).

(b) (i) Very few identified both components. Answers such as "glass fibre" and "insulation" were common.

(ii) Too many attempted to use technical language but used it incorrectly - "…Y has a greater refractive index than X…", "…angle of incidence… less than the critical angle…".

(c) (i) This was not well-answered. The characteristic curve showed that the output saturated at +10 V and -10 V and that switching took place at threshold voltages of +8 V and -8 V. Few knew how to translate this information into a Schmitt trigger design.

(ii) Generally well answered. The horizontal axis should have been labelled ‘Time’, this was taken into consideration when marking.

Summary of key points

- Candidates must show all workings for calculations.
- Candidates must be able to expand multipliers.
- Candidates should read the question carefully, paying particular attention to the verb:
- “Describe…” / “Explain…” / “State…” etc.
- Candidates should use a pencil and ruler for all diagrams.

ELECTRONICS

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COMPONENT 3: SYSTEM DESIGN AND REALISATION TASKS - NEA

General Comments

Centres are to be congratulated for their effort in presenting candidates' work for moderation, including the online recording of centre marks.

The assessment of the work was within tolerance in the vast majority of centres but in a small number of centres adjustments to marks were required.

Candidates should focus on a problem to analyse to enable them to write a design specification based on a specific identified problem.

Many candidates struggled to provide meaningful parameters and simply quoted power supply values, current consumption and cost without any justification. A full specification should include measurable parameters and numerical data.

Candidates in the majority of centres provided excellent photographic evidence.

Annotation of candidates' work was quite limited. A large number of centres failed to provide any annotation. An indication on the mark scheme of which level descriptors were or were not achieved would greatly aid the moderation process.

All circuits are required to be constructed using breadboard, stripboard or printed circuit board. The use of development boards is not acceptable for final circuits.

A common weakness in both tasks was in the **Evaluation** section.

To gain the full range of marks for the evaluation candidates must make valid, critical and objective evaluation of the performance of the complete system. The evaluation should compare the system against the design specification.

A common problem was that the consequence of not having many measurable parameters in the specifications resulted in some simplistic evaluations.

Suggestions for improvement must be relevant and should state why incorporating such an improvement would be beneficial.

Comments on individual questions/sections

Task 1

For the microcontroller task at A level, candidates are required to program the microcontroller using assembly language, other programming languages are not acceptable. A small number of centres allowed candidates to produce hybrid programs that included both assembler and Basic commands. (This is possible within PICAXE but not within the MPLAB environment).

A number of centres submitted microcontroller projects containing light sequences resulting in all candidates within the centre producing very similar programs. As the tasks are from individual problems identified by the candidates it would be expected that specification parameters would usually be different, and programs have variations in structure and commands used.

Some candidates used the PICAXE programming environment produced programs which called delay sub-routines 'wait100ms' and ‘wait1000ms'. These were not listed in the template provided. All standard sub-routines are listed in the ‘Assembly Language Template’ provided on EDUQAS website. Any sub-routines called and equate statements used should be included in the task 1 template. It is important that candidates realise that these sub-routines and equate statements actually exist.

Credit cannot be awarded for commands used to configure the ports. However, credit can be given should these same commands be used by the candidate in their main program and any sub-routine they write.

Task 2

The specification requires candidates to select their own focus for the tasks based on different problems and this is expected to produce a wide range of tasks within a centre. The range of tasks produced within centres was variable. In many centres’ candidates produced a very good range of tasks with some of the work being outstanding and demonstrating considerable innovation. In a very small number of centres all candidates produced projects that tended to consist of several unrelated and separate circuits. A project should consist of a number of sub-systems that are interconnected and have signals that are transferred from one sub-system to another.

Design specifications should contain a range of both qualitative and quantitative terms based on their analysis of the problem and contain detailed realistic electronic parameters.
A common misconception was to identify sub-systems and/or components as part of the specification. The choice of a particular sub-system/component may be part of the design solution to a problem but would not normally be part of the specification.

A significant number of candidates provided extensive photograph evidence showing voltmeter reading at various stages of system development. Although this is useful it should be considered as a supplement to tabulated results rather than an alternative.
Even when tabulated test results were provided there was often very little analysis of the results.

Page 39 of the A level specification clearly states that 'Pre-constructed circuit boards such as PIC or Arduino development boards are not acceptable as the final circuit' and Page 38 states 'The tasks build on the concepts studied throughout the specification and the requirements to relate practical circuit design and realisation to knowledge and understanding gained from the study of components 1 and 2.' For tasks using microcontroller, candidates are expected to program the microcontroller via a flowchart program or assembly language. Programs written in C+ or other high-level languages are not acceptable as they would form a major part of a system and not allow the tasks to access the candidate’s knowledge and understanding of the specification.

To access the full range of marks for system realisation the use of an appropriate instrument is expected. For example, measuring the mark/space ratio of an astable circuit with an oscilloscope.

On the whole the physical circuit layout produced by candidates was of a good standard. The majority of the work was constructed on breadboard.

Summary of key points

- Candidates should focus on a problem to analyse to enable them to write a design specification based on a specific identified problem. Good analysis of a problem should enable candidates to provide meaningful parameters with clear justification, including measurable parameters and numerical data.

- Candidates must make valid critical and objective evaluation of the performance of the complete system, comparing the system against the design specification. Candidates' suggestions for improvement must be relevant.

- Task 1: microcontroller system, candidates are required to program the microcontroller using assembly language, other programming languages are not acceptable, this includes hybrid programs that are only part assembler (assembler and Basic commands).

- Test results should be tabulated, and the results should be analysed against intended performance of the sub-system/system.

- The majority of Task 2: Electronic system design should fall within the A level specification to allow for the assessment of the candidate's knowledge and understanding of the specification.

- Pre-constructed circuit boards such as PIC or Arduino development boards are not acceptable as the final circuit.

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